Description

• Introduction to HDL basic elements, HDL simulation concepts, HDL concurrent statements with examples and applications, writing HDL for synthesis, and writing HDL for finite state machines.

• In this course, we will teach Verilog HDL.

• You will learn the design techniques and methodologies employed in the industry.

• This course prepares you to be a logic designer or a verification engineer.
Prerequisites

• ECE 152A Digital Design Principles

• You should be familiar with the material covered in ECE 152A such as
  - boolean algebra, switching functions, application of Boolean algebra to the design and analysis of combinational logic nets, minimization procedures, analysis and synthesis of sequential switching circuits, synchronous and asynchronous operation, state minimization, hazards, and races.
Textbooks

  - You can order online
  - Or buy it from the bookstore

  - Not absolutely required
  - But this is an excellent book to learn about the foundation of Synthesis processes
Verilog Tool

- For Verilog simulation, we recommend you to use Mentor Graphics ModelSim in the ECI lab
  - Get an account from ECI lab
  - Login from home with window display
  - Very handy for experienced user
Using Design Compiler

• You can use any Verilog simulator to check the correctness of your Verilog code
  – But if there is any discrepancy, we will use ModelSim as the golden reference for correctness

• Later in the quarter, I will introduce you the synthesis tool, Design Compiler (DC)
  – There will be 1 or more exercises using DC
  – You will need an account at the ECI lab
  – Please open an account at the ECI lab if you haven’t had one
  – TAs will give a tutorial on DC later
Web Site

• My home http://mtv.ece.ucsb.edu/

• Course web page
  http://mtv.ece.ucsb.edu/courses/ece156A_13/
    - No need for Username and Password
    - The update of course web page may be delayed from time to time.
    - Please be patient.
Grading

• Homework and Programming Assignments
  – 40%
  – About 6-7 of them
  – Entirely controlled and graded by TAs

• Two Exams
  – In-class Mid-term: 30%, Nov 13th, Wednesday
  – Final: 30% (as scheduled by the school)
  – Both are closed-book exams
  – No exception on exam times and formats
Special Schedule

• Attending conference
  – Nov 18, Monday (no class)

• Instruction ends on December 4 (Wed)

• I will be out of town during Dec 9-11
  – TAs will be there for the final exam
TAs and Lab sessions

• Lab R 9-11:50am
  - Wei Dai
  - weidai@umail.ucsb.edu
  - Office hour:

• Lab R 5-7:50pm
  - Amirali Ghofrani
  - amirali.ghofrani@gmail.com
  - Office hour:

• Lab T 5-7:50pm
  - Sebastian Siatkowski
  - ssiatkowski@umail.ucsb.edu
  - Office hour:

• My office hour – before and after the class
Lab sessions and grading

- **One lab session for every HW assignment**
  - TA will instruct you about the lab session
  - We don’t have lab session every week

- **Homework grading**
  - Turn in your HW to your TA
  - Your TA will grade them

- **Discussion group**
  - Each lab session will form a discussion group
  - Your TA will send you an email about the group
Intended Course Outline

- Overview of design methodology (Chap 1)
  - Self-review: Chap 2 and Chap 3
- Introduction to Verilog (Chap 4)
- Behavior modeling (Chap 5)
- Introduction to synthesis (Chap 6)
- 2-level logic synthesis (2\textsuperscript{nd} textbook)
  - Traditional method
  - Complete sum method
  - Solving constraint matrix problem
- Functional verification
- Postsynthesis design task (Chap 11)
  - Static timing analysis
Five Questions

• Why am I here?

• What do I expect to learn?

• What am I going to do next year?

• How can being here help me?

• What do I not understand?
10 Points We Might Learn

• 10 Design means “constrained optimization”
• 9 Design is based on models and models are not reality and they are never 100% correct
• 8 No perfect design; you just need to be better than your competitor
• 7 It is all about efficiently handling the complexity
• 6 More important to put yourself into the right vision and perspective
• 5 When searching for a solution in a complex space, it is more effective to know where you don’t have a solution
Cont.

• 4 Understand your problem well, then the solution will come to you
• 3 When something does not make an intuitive sense, it probably does not make sense
• 2 All practical answers are simple; Only simple answers are practical
• 1 There is no difficult problem; If you find it difficult, the difficulty is only reflecting something about yourself