Sean Hsi Yuan Wu

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OBJECTIVE:

- To obtain a challenging position relates to following field relates but not limited to: Statistical data mining/analysis, Design for Test (DFT), design methodology, test methodology, yield learning/improvement, defect diagnosis, quality engineering, project management, and/or a field where I can contribute, learn, and grow with the organization. Work Status: US Citizen

EDUCATION:

University of California, Santa Barbara, USA

- **Ph.D Program.** *Department of Electrical and Computer Engineering*, 01/05' – 03/09' GPA: 3.81. Thesis title: "Dealing with Test Issues in Typical ASIC Design Flow."
- **M.S.** *Department of Electrical and Computer Engineering*, emphasize in VLSI, 09/03' – 01/05' GPA: 3.73
- **B.S.** *Department of Electrical and Computer Engineering*, emphasize in communication device design, 09/99' – 09/03' GPA: 3.45

TECHNICAL SKILLS:

- Excellent communication skill, strong team player, capable individual contributor, fast learner
- Experience with Unix/Windows OS, Agilent Logic Analyzers, Oscilloscopes, and Network Analyzers
- Familiarity with R, Perl, Python, C/C++, MATLAB, and Mathmatica.
- Experience with Advanced Design System (ADS), HSPICE, and ModelSim
- Some experience with ATPG tool Fastscan, Spectre, Tcl, Assembly, and Verilog
- Some experience with Synopsys Primetime, Cadence QRC, and Magma design flow
- Classroom experience in clean room of semiconductor fabrication
- Fluent in English and Chinese (Mandarin)

EXPERIENCE:

LSI Corp., Milpitas, CA

Contract Engineer, Power, Package and Test group**, 05/07' - present**

Impact of On Chip Variation (OCV) on Timing Sign-off Methodology

- Studied OCV could affect designs on 90 and 65nm standard cell libraries
- Discovered design sign-off methodology flaw against invert temperature dependency
- Proposed solution on design sign-off methodology to achieve more robust design
- Analyzed and assisted in developing test structure in 45nm fabrication to study impact of variations and design-silicon correlation

Delay Test Methodology

- Improved delay test methodology to identify longest paths in 65nm and 45nm designs that consist of standard cells with asymmetrical transition delays
- Improved in-line resistance fault model for guiding test optimization
- Selected tests are more effective up to 30% comparing with earlier scheme

Defect Screening Methodology

- Proposed new analysis method to lower overkill rate by 50% comparing to current method

Dept of ECE, University of California, Santa Barbara, CA

Research Assistant, Microprocessor Testing and Validation Lab, **01/05' – present**

Post-Silicon Data Mining (SVM and Random Forests)

- Extracted the non-obvious trend from test data to guide test optimization
- Introduced probabilistic pass/fail decision for yield recovery and risk management based on cost model with more advance data analysis algorithm
- Successfully screened out unreliable samples, that escaped traditional test methodology, using novel data mining algorithms in early test flow

Standard Cell Characterization

- Built standard cell timing library with Hspice for in-house statistical timing analyzer on designs

Analog Data Mining

- To build fast and accurate prediction model from result of slow simulation tool
- Conducted preliminary study on data mining on analog simulation data

CNet Technology, Hsinchu, Taiwan 06/03' – 08/03'

- **Intern R/D Engineer,** 802.11b WLAN Card design optimization team.
  - Optimized, implemented, and tested the WLAN Card design; analyzed antenna performance to increase the signal strength

PUBLICATION:

Conference

- **Sean Wu,** Sreejit Chakravarty, and Li-C. Wang, *Study of the Impact of Multiple Input Switching on Speed Binning Using Path Delay Tests.* Submitted to IEEE International Test Conference 2009 (ITC'09)
- **Sean Wu,** Sreejit Chakravarty, Alexander Tetelbaum, and Li-C. Wang. *Refining Delay Test Methodology Using Knowledge of Asymmetric Transition Delay*. IEEE Asian Test Symposium 2008 (ATS'08)
- **Sean Wu,** Dragoljob (Gagi) Drmanac, and Li-C. Wang. *A Study of Outlier Analysis Techniques for Delay Testing*. IEEE International Test Conference 2008 (ITC'08).
- **Sean Wu,** Alexander Tetelbaum, Li-C. Wang. *How Does Inversed Temperature Dependence Affect Timing Sign-off.* IEEE International Conference on IC Design and Technology 2008 (ICICDT'08).
- **Sean Wu,** Alexander Tetelbaum, Pouria Bastani, and Li-C. Wang. *Impact of Temperature Inversion on Timing Sign-off and Design Methodology*. Presented in Microprocessor Test and Validation Workshop 2007 (MTV07')
- **Sean Wu**, Benjamin N Lee, Li-C Wang and Magdy Abadir. *Statistical Analysis and Optimization of Parametric Delay Testing.* IEEE International Test Conference 2007 (ITC'07).
- Leonard Lee, **Sean Wu**, Charles H.-P. Wen, and Li-C. Wang. *On Generating Tests to Cover Diverse Worst-Case Timing Corners*. in IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, pp. 415-423, Oct. 3-5, 2005.

OTHER EXPERIENCE:

Paper and Journal reviewer, review paper and journal submission for various conferences and journals in field of IC testing and design methodology.

Conference/Workshop Planning

- Semiconductor Research Corp. Test Review 2006
- International Test Synthesis Workshop 2007
- Local arrangement committee for VLSI Test Symposium(VTS) 2009
- Arranged local facility, lodging, meals, and transportation; negotiate and coordinate with vendors for deals and on-field issues

REFERENCES: Prof. Li-C. Wang (licwang@ece.ucsb.edu);
Dr. Kenneth M. Butler (kenb@ti.com); others upon request