LI-C. WANG
Professor
Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106-9560

CONTACT: Email: licwang@ece.ucsb.edu, Phone: 805-886-6017

EDUCATION:

Ph.D. Electrical and Computer Engineering, University of Texas, Austin, May 1996
Master of Science in Computer Sciences, University of Texas at Austin, December 1991
B.S. in Computer Engineering, National Chao-Tung University, May 1986

COURSES TAUGHT at UCSB:

ECE 156A Digital Design with VHDL and Synthesis (undergraduate) – every Fall quarter since 2001
ECE 156B Computer-Aided Design of VLSI (undergraduate) – Spring quarter 2003, and every Winter quarter since 2004
ECE 255B VLSI Design Validation (graduate) – Winter quarter 2002 and 2003, and every Spring quarter since 2004 until 2013, winter quarter 2015
ECE 255A VLSI Testing Techniques (graduate) – Spring quarter 2014
ECE 154 Introduction to Computer Architecture (undergraduate) – Winter quarter 2001
ECE 15B Computer Organization (undergraduate) – Spring quarter 2001 and 2003

PIROR INDUSTRIAL APPOINTMENTS:

Software engineer, Motorola, Inc., Austin, Texas, 1/99-12/00 (part-time)
Software engineer, Motorola, Inc., Austin, Texas, 3/96-12/98
Technical Staff, Mathematics Research, AT&T Bell Labs, Murray Hill, NJ, 91-95 summers

PRIOR ACADEMIC APPOINTMENT:

Associate Professor, Department of Electrical and Computer Engineering, University of California, Santa Barbara, Summer/2004-Summer/2010
Assistant Professor, Department of Electrical and Computer Engineering, University of California, Santa Barbara, Jan/2001-Summer/2004
Assistant Professor, Department of Electrical Engineering, Texas A&M University, College Station, Texas, Spring/99-Fall/00

PROFESSIONAL ACTIVITIES:

Guest Co-editors

- IEEE Design & Test of Computers, special issue on *Speed Test and Speed Binning for complex ICs*, Sept-Oct, 2003
- IEEE Design & Test of Computers, special issue on *Functional Verification and Testbench Generation*, March-April, 2004
- IEEE Design & Test of Computers, special issue on *Advances in Functional Validation through Hybrid Techniques*, March-April 2007
- ACM Transactions on Design Automation of Electronics Systems, on *Verification Challenges in the Concurrent World*, 2012
- Journal of Electronic Testing, on *Test and Verification Challenges for Future Microprocessors and SoC Designs*, 2013

Editorial Service

- **Associate Editor**, IEEE Transactions on Computer-Aided Design of Integrated Systems (TCAD), 2011 to 2015

Technical Program Committee Track Chair/Program Co-Chair

- **Technical Program Co-Chair**, IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2012 and 2013
- **Technical Program Chair/Co-Chair**, IEEE International Workshop on Microprocessor Test and Verification (MTV), 2002 to 2015
- **Technical track chair**, IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Test and Verification track, 2008 to 2011
- **Technical Track Chair**, IEEE International Symposium on Quality of Electronic Design (ISQED), Design for Verification and Test (DFVT) track, , 2003 to 2011
- **Track Chair in test area**, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2010 to 2011

Technical Program Committee

- IEEE VLSI Test Symposium (VTS), 2002 to 2005, 2013 to 2015
- IEEE Asian Test Symposium (ATS), 2004 to 2005, 2008, 2010, 2011, 2013 and 2014
- IEEE International Test Conference (ITC), 2007 to 2015
- ACM/IEEE Design Automation Conference (DAC), 2014 and 2015
- IEEE/ACM European Design Automation and Test Conference (DATE), 2008 to 2009, 2014 and 2015
- ACM/IEEE Great-Lake VLSI Test symposium, 2015
- ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2009
- IEEE International On-line Test Symposium, 2009 to 2011
- IFIP/IEEE International Conference on VLSI, 2014
- Haifa Verification Conference, 2012 and 2013
- IEEE International Conference on Computer Design (ICCD), 2004 to 2006
- IEEE International High-Level Design Validation and Test Workshop (HLDVT), 2003 to 2010
- ACM SIGDA Technical Committee on Verification, 2009

Organizing Committee/General Chair

- **General Co-Chair**, IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2014 and 2015
- **Organizing Committee**, IEEE VLSI Test Symposium (VTS), 2009 to 2011
- **Organizing Committee**, IEEE International High-Level Design Validation and Test Workshop (HLDVT), 2008
- **Steering and organizing committee**, IEEE International Test Synthesis Workshop, 2001 to 2010

AWARDS AND HONOR:

Technical Excellence Award, Semiconductor Research Corporation (www.src.org), 2010
Best Paper Award, IEEE International Symposium on VLSI Design, Automation and Test, 2011
Best Student Paper Award, IEEE International Symposium on VLSI Design, Automation and Test, 2008
Best Paper Award, Design Automation and Test in Europe (DATE) 2003
Best Paper Award, IEEE VLSI Test Symposium (VTS) 1999
Best Paper Award, European Design Automation and Test Conference (DATE) 1998
Best Paper Award Candidate, ACM/IEEE Design Automation Conference (DAC), 2008 and 2010

Best Paper Award Candidate, ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC) 2003
Best Panel Award**,** IEEE VLSI Test Symposium (VTS) 2003

TUTORIALS GIVEN:

- **On Data Ming/Big Data Analytics for Design Automation and Test**
  - "*Big Data Analytics in VLSI Design Automation and Test – Principles, Challenges, and Promises*" (Full-day tutorial at National Tsing-Hua University, Taiwan, April 2015)
  - "*Data Mining in Design & Test - Principles and Practices*" (Half day tutorial presented at National Cheng-Kung University, Tainan, Taiwan, May 2014)
  - "*Data Mining in Design & Test - Principles and Practices*" (Half day tutorial presented at Industrial Technology Research Institute (ITRI), HsinChu, Taiwan, November 2013)
  - "*Data Mining in Design & Test - Principles and Practices*" (Full day tutorial presented at Intel Corporation, Hillsboro, OR, October 2013)
  - "*Data Mining in Design & Test - Principles and Practices*" – April 2014
    (**Click the title to download the PowerPoint slides**)
    (Half day tutorial presented as a special event for IEEE CEDA/Austin Texas chapter)
  - "*Data Mining in Test - Principles and Practices*" (3-hour tutorial presented at IEEE Asian Test Symposium, 2013)
  - "*Data Mining in Test & Verification - Principles and Practices*" (Half day tutorial presented at IEEE International Test Conference, 2013 as part of IEEE TTEP tutorial program; Co-Presenter: Magdy S. Abadir)

- **Timing analysis, validation and post-silicon timing validation**
  - "*Dealing with timing issues for sub-100nm designs*"
    (Full day tutorial presented at IEEE International Test Conference 2005, 2006 and 2007;
    Full day tutorial presented at IEEE VLSI Test Symposium, 2007;
    as part of the IEEE TTEP tutorial program; Co-Presenter: Magdy S. Abadir)

- **Microprocessor Verification and Validation**
  - "*Validation and Verification of High-Performance Microprocessors and Socs: Challenges and Solutions*" (Full day tutorial presented at IEEE International Test Conference, 2003, as part of the IEEE TTEP tutorial program; Co-Presenter: Magdy S. Abadir)
  - "*Validation and Verification of Complex Digital Systems -- A Practical Perspective*" (Full day tutorial presented at IEEE International Test Conference, 2001, as part of the IEEE TTEP tutorial program; Co-Presenter: Magdy S. Abadir)
  - "*Validation and Verification of Complex Digital Systems – An Industrial Perspective*" (Half day tutorial presented at International Symposium on Quality of Electronic Design (ISQED), 2001
  - "*Validation and Verification of Complex Digital Systems -- A Practical Perspective*" (Full day tutorial presented at IEEE VLSI Test Symposium, 2001, as part of the IEEE TTEP tutorial program; Co-Presenter: Magdy S. Abadir)

- **Formal Verification**
  - "*Recent Advances in Verification: Equivalence Checking and SAT Solvers*" – tutorial B.1, European Design and Test Conference (DATE), 2003 (As part of the IEEE TTEP tutorial program; Lead-Presenter: Dhiraj Pradhan, Magdy S. Abadir)

LECTURES AND PRESENTATIONS:

- **Data Mining in Design Automation and Test**
  - "*Machine Learning in Simulation Based Analysis*" at ACM/IEEE International Symposium on Physical Design (ISPD), 2015
  - "*Data Mining in Functional Test Content Optimization*" at IEEE Asian South Pacific Design Automation Conference, Jan 2015
  - "*Data Mining in EDA - Basic Principles, Promises, and Constraints*" at ACM/IEEE Design Automation Conference, 2014
  - "*Data Mining in Design and Test Processes - Basic Principles and Promises*" at ACM/IEEE International Symposium on Physical Design (ISPD), 2013
  - "*Data Mining Research and Applications in Test & Verification*" at Intel Corporation, June 2012
  - "*Mining Test Data and Applications*" at MediaTek, Inc. HsinChu, Taiwan, April 2012
  - "*Multivariate Approaches for Learning Parametric Test Data*" at Qualcomm, San Diego, Aug 2011
  - "*Knowledge discovery in design and test data*" at SRC eWorkshop, Aug 2010
  - "*Gaps & research vectors In SOC validation & test - a data mining perspective*" at Intel Corporation, Nov 2010
  - "*Data learning based diagnosis*" at Asian South Pacific Design Automation Conference (ASP-DAC), Jan 2010
  - "*Data mining and machine learning - applications in test, diagnosis, and more*" at DT3 workshop with International Test Conference, Nov 2010
  - "*Mining Test Data and Applications*" at AMD, Austin, Texas, May 2010
  - "*Knowledge Discovery in Test Data*" at Freescale Semiconductor Inc., Austin, Texas, May 2010
  - "*Model-to-hardware Correlation - Design Automation Perspective*" at Smart Grid Workshop with Design Automation Conference 2010, June 2010
  - "*Kernel based learning for simulation efficiency*" at National Tsing-Hua University, HsinChu, Taiwan, Dec 2008
  - "*Data learning framework for diagnosis based yield optimization*" at National Chiao-Tung University, HsinChu, Taiwan, Dec 2008
  - "*Data learning framework for diagnosis based yield optimization*" at National Cheng-Kung University, Tainan, Taiwan, Dec 2008
  - "*A path-based learning framework for learning design-related information*" at SRC eWorkshop, July 2008
  - "*Simulation data mining for functional verification*" at AMD, Austin, Texas, April 2008
  - "*Closing design-silicon timing gap by learning from a set of paths*" at IBM Austin Research Center, Austin, Texas, Dec 2007
  - "*Timing risk evaluation - A statistical perspective*" at LSI Corporation, Milpitas, CA, July 2007
  - "*Finding answers and making decisions based on test data - a statistical perspective*" at IBM T J Watson Research Center, New York, July 2007
  - "*Design-Silicon Timing Correlation --- A Data Mining Perspective*" at AMD Austin Design Center, Austin, Texas, Feb 2007
  - "*Fining Answers in Test Data - from diagnosis to statistical data mining*" at Strategy CAD Lab, Intel Corporation, Hillsboro, Oregon, Jan 2007
  - "*Dealing with timing dependent effects in the presence of timing variation*" at Test Technology, Intel Corporation, Santa Clara, California, Sep 2006
  - "*Applications of Learning Algorithms in Statistical Testing*" at National Tsing-Hua University, HisnChu, Taiwan, Aug 2006
  - "*Dealing with Timing - A Statistical Perspective*" at Mentor Graphics Corporation, Oregon

- "*Simulation data mining for functional test pattern justification*" at National Tsing-Hua University, HisnChu, Taiwan, Dec 2005
- "*Simulation data mining for functional test pattern justification*" at Freescale, Austin, Texas, Sep 2005

- **Speed test, delay test and performance validation**
  - "*Statistical Timing Tools and Methodologies for Speed Test and Performance Validation*" at Texas Instruments, Dallas, Texas, Oct 2005
  - "*Statistical Timing Tools for Speed Test and Validation*" at IBM Austin Research Center, Austin, Texas, July 2005
  - "*Statistical Timing Tools and Methodologies for Speed Test and Performance Validation*" at Stanford University, Center for Reliable Computing, July 2005
  - "*Test with variations*" at LSI Logic, Dec 2004
  - "*Test with variations*" at ECE department, USC, Dec 2004
  - "*Statistical Tools and Methodologies For Delay Test and Timing Validation*" at Department of EE, University of Washington, Seattle, May 2003
  - "*Statistical Tools and Methodologies For Delay Test and Timing Validation*" at Department of Electrical Engineering, University of Southern California, May 2003
  - "*Statistical Tools and Methodologies For Delay Test and Timing Validation*" at UC-Irvine, May 2003
  - "*Statistical Frameworks For Delay Test and Timing Validation*" at Intel Austin Design Center, Austin, TX, June 2002
  - "*Statistical Frameworks For Delay Test and Timing Validation*" at Agilent, San Jose, CA, June 2002
  - "*Statistical Frameworks For Delay Test and Timing Validation*" at Texas Instruments, Dallas, TX, June 2002

PHD STUDENTS SUPERVISED:

1. Tao Feng (Google) - 2003
2. Leonard Lee (Cadence) - 2005
3. Ben Lee (startup) - 2006
4. Charles H.P. Wen (National Chao-Tung Univ., Taiwan) - 2006
5. Pouria Bastani (Intel) - 2008
6. Onur Guzey (Istanbul Sehir U., Turkey) - 2008
7. Sean Wu (TPK, Taiwan) - 2008
8. Nick Callegari (nVidia)) - 2009
9. Hui Li (Intel) - 2010
10. Po-Hsien Chang (Oracle) - 2011
11. Janine Chen (AMD) - 2010
12. Gagi Drmanac Intel) - 2011
13. Nik Sumikawa (Freescale) - 2013
14. Vinayak Kamath (AMD) - 2014
15. Wen Chen (Freescale) - 2014
16. Samatha Alt (Intel) - 2014

PUBLICATIONS:

More than 140 papers published in the areas of electronic design automation and test.

According to Google Citation Indices

- Citations: 2135
- h-index: 27 (27 papers each with at least 27 citations)

A. Recent Invited Papers on Data Mining

[1] "*Machine Learning in Simulation Based Analysis*"
Li-C. Wang and Malgorzata Marek-Sadowska,
2015 ACM/IEEE International Symposium on Physical Design (ISPD), 8 pages

[2] "*Data Mining in Functional Test Content Optimization*"
Li-C. Wang,
2015 ACM/IEEE Asian South Pacific Design Automation Conference (ASP-DAC), 8 pages.

[3] "*On Application of Data Mining in Functional Debug*"
Kuo-Kai Hsieh, Wen Chen, Li-C. Wang, Jayanta Bhadra
2014 ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 8 pages

[4] "*Data Mining in EDA – Basic Principles, Promises, and Constraints*"
Li-C. Wang and Magdy S. Abadir,
2014 ACM/IEEE Design Automation Conference, pp 1-6.

[5] "*Data Mining in Design and Test Processes – Principles and Promises*,"
Li-C. Wang,
2013 IEEE International Symposium on Physical Design (ISPD), pp 41-42

B. Data Mining for Design-Silicon Timing Mismatch Analysis and Speedpath analysis

(a) Design-Silicon Timing Mismatch Analysis

[6] "Mining AC Delay Measurements for Understanding Speed-limiting Paths"
Janine Chen, Brendon Bolin, Li-C. Wang, Jing Zeng, Dragoljub (Gagi) Drmanac, and Michael Mateja,
2010 IEEE International Test Conference, 2010, pp 1-10.

[7] "Classification rule learning using subgroup discovery of cross-domain attributes responsible for design-silicon mismatch"
Nicholas Callegari, Dragoljub (Gagi) Drmanac, Li-C. Wang, Magdy S. Abadir,
2010 ACM/IEEE Design Automation Conference (DAC), pp 374-379
(**Nominated for Best Paper Award**)

[8] "Feature-Ranking Methodology to Diagnose Design-Silicon Timing Mismatch"
Pouria Bastani, Nick Callegari, Li-C.Wang, Magdy S. Abadir,
2010 IEEE Design & Test, Volume 27, Issue 3, May-June 2010, pages 42-53

[9] "Data Learning Based Diagnosis"
Li-C. Wang,
2010 ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), pages 247-254

[10] "A Statistical Diagnosis Approach Analyzing Design-Silicon Timing Mismatch"
Nicholas Callegari, Pouria Bastani, Li-C. Wang, Magdy Abadir,

2009 IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD), Volume 28, Issue 11, Nov. 2009, Pages 1728-1741

[11] "Diagnosis of design-silicon timing mismatch with feature encoding and importance ranking – the methodology explained"
Pouria Bastani, Nick Callegari, Li-C.Wang, Magdy S. Abadir,
2008 IEEE International Test Conference (ITC) 2008, pp. 1-10.

[12] "Statistical Diagnosis of Unmodeled Systematic Timing Effects"
Pouria Bastani, Nicholas Callegari, Li-C. Wang, Magdy S. Abadir,
2008 ACM/IEEE Design Automation Conference, June 2008, pages 355-360.

[13] "Linking Statistical Learning to Diagnosis"
Bastani, Pouria; Wang, Li-C; Abadir, Magdy S.,
2008 IEEE Design & Test of Computers, Vol 25, Issue 3, pages 232-239.

[14] "An Improved Feature Ranking Method for Diagnosis of Systematic Timing Uncertainty"
Pouria Bastani, Nicholas Callegari, Li-C. Wang, Magdy Abadir
2008 IEEE International Symposium on VLSI Design, Automation, and Test, HsinChu, Taiwan, pages 101-104. (**Best Student Paper Award**)

[15] "Analyzing the risk of timing modeling based on path delay tests"
Bastani, Pouria; Lee, Benjamin N.; Wang, Li-C.; Sundareswaran, Savithri; Abadir, Magdy S.,
2007 IEEE International Test Conference, pp. 1-10. Digital Object Identifier 10.1109/TEST.2007.4437587

[16] "Design-Silicon Timing Correlation --- A Data Mining Perspective"
Li-C. Wang, Pouria Bastani, Magdy S. Abadir,
2007 ACM/IEEE Design Automation Conference (DAC), June, 2007, pp 384-389

(b) Post-Silicon Speedpath Analysis

[17] "*Feature based similarity search with application to speedpath analysis*"
Nicholas Callegari, Li-C. Wang, Pouria Bastani,
2009 IEEE International Test Conference (ITC), pp. 1-10.

[18] "*Speedpath Analysis Based on Hypothesis Pruning and Ranking*"
Nicholas Callegari, Li-C. Wang, Pouria Bastani,
2009 ACM/IEEE Design Automation Conference, pp. 346-351.

[19] "*Path selection for monitoring unexpected systematic timing effects*"
Nicholas Callegari, Pouria Bastani, Li-C.Wang, Sreejit Chakravarty, Alexander Tetelbaum,
2009 ACM/IEEE Asia and South Pacific Design Automation Conference, pages 781-786.

[20] "*Speedpath Prediction Based on Learning from a Small Set of Examples*"
Pouria Bastani, Kip Killpack, Li-C. Wang, Eli Chiprout,
2008 ACM/IEEE Design Automation Conference, June 2008, pages 217-222.
(**nominated for the Best Paper Award**)

C. Data Mining in RTL Functional Verification

(c) Reducing Simulation Cost

[21] "*Novel Test Detection to Improve Simulation Efficiency – A Commercial Experiment*"
Wen Chen, Nik Sumikawa, Li-C. Wang, Jayanta Bhadra, Xiushan Feng, Magdy S. Abadir,
2012 ACM/IEEE International Conference on Computer-Aided Design, pp. 101-108

[22] "*Novel Test Analysis to Improve Structural Coverage*"
Wen Chen, Li-C. Wang, Jayanta Bhadra, Magdy Abadir,
2013 International Symposium on VLSI Design Automation and Test (VLSI-DAT), pp 1-4.

[23] "*Online Selection of Effective Functional Test Programs Based on Novelty Detection*"
Po-Hsien Chang, Dragoljub (Gagi) Drmanac, and Li-C. Wang,
2010 IEEE/ACM Intern'l Conference on Computer-Aided Design (ICCAD), pp 762-769.

[24] "*A Kernel-Based Approach for Functional Test Program Generation*"
Po-Hsien Chang, Li-C. Wang, Jayanta Bhadra,
2010 IEEE International Test Conference, pp. 1-10.

[25] "*Increasing the efficiency of simulation-based functional verification through unsupervised support vector analysis*"
Onur Guzey, Li-C. Wang, Jeremy Levitt, Harry Foster ,
2010 IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD),
Volume 29, Issue 1, Jan 2010, Pages 138-148

[26] "*Functional Test Selection Based on Unsupervised Support Vector Analysis*"
Onur Guzey, Li-C. Wang, Jeremy Levitt, Harry Foster,
2008 ACM/IEEE Design Automation Conference, June 2008, pages 262-267.

(d) Improving Test Content and Coverage

[27] "*Simulation Knowledge Extraction and Reuse in Constrained Random Processor Verification*"
Wen Chen, Li-C. Wang, Jayanta Bhadra,
2013 ACM/IEEE Design Automation Conference, pp 1-6.

[28] "*Functional Test Content Optimization for Peak-Power Validation - An Experimental Study*"
Vinayak Kamath, Wen Chen, Nik Sumikawa, Li-C. Wang,
2012 IEEE International Test Conference (ITC), 10 pages

[29] "*Coverage-directed test generation through automatic constraint extraction*"
Guzey, O.; Wang, L.-C.,
2007 IEEE International Workshop on High Level Design Validation and Test (HLDVT)
Page(s): 151-158

D. Machine Learning in Layout Hot-Spot Prediction

[30] "Predicting Variability in Nanoscale Lithography Processes"
Dragoljub (Gagi) Drmanac, Frank Liu, Li-C. Wang,
2009 ACM/IEEE Design Automation Conference, July 2009, pp. 545-550.

E. Data Mining for Yield, Test Cost, and Customer Return Analysis

(e) Yield

[31] "*Yield Optimization Using Advanced Statistical Correlation Methods*"
Jeff Tikkanen, Sebastian Siatkowski, Nik Sumikawa, Li-C. Wang and Magdy S. Abadir,
2014 IEEE International Test Conference (ITC), 10 pages

(f) Customer Return Analysis

[32] "*Multivariate Outlier Modeling for Capturing Customer Returns – How Simple It Can Be*"
Jeff Tikkanen, Nik Sumikawa, Li-C. Wang, Magdy S. Abadir,
2014 IEEE On-Line Test Symposium, pp 164 – 169

[33] "*A Pattern Mining Framework for Inter-Wafer Abnormality Analysis*"
Nik Sumikawa, Li-C.Wang, Magdy S. Abadir,
2013 IEEE International Test Conference (ITC), 10 pages

[34] "Screening Customer Returns With Multivariate Test Analysis"
Nik Sumikawa, Li-C.Wang, LeRoy Winemberg, and Magdy S. Abadir,
2012 IEEE International Test Conference (ITC), 10 pages

[35] "Statistical Outlier Screening for Latent Defects"
Jeff Tikkanen, Nik Sumikawa, Li-C.Wang, LeRoy Winemberg,
2013 IEEE International Symposium on Reliability Physics (IRPS), pp. 2E 1.1-1.4

[36] "Forward Prediction Based on Wafer Sort Data – A Case Study"
Nik Sumikawa, Dragoljub (Gagi) Drmanac, Li-C.Wang, LeRoy Winemberg, and Magdy S. Abadir
2011 IEEE International Test Conference (ITC), 10 pages

[37] "Important Test Selection For Screening Potential Customer Returns"
Nik Sumikawa, Dragoljub (Gagi) Drmanac, LeRoy Winemberg, Li-C. Wang and Magdy S. Abadir,
2011 VLSI Design Automation and Test Symposium, pages 171-174. (**Best Paper Award**)

[38] "Understanding Customer Returns From A Test Perspective"
Nik Sumikawa, Dragoljub (Gagi) Drmanac, Li-C.Wang, LeRoy Winemberg, and Magdy S. Abadir,
2011 IEEE VLSI Test Symposium (VTS), April 2011, Pages 2-7.

(g) Test Cost

[39] "An Experiment of Burn-In Time Reduction Based On Parametric Test Analysis"
Nik Sumikawa, Li-C.Wang, Magdy S. Abadir,
2012 IEEE International Test Conference (ITC), 10 pages

[40] "Multidimensional Parametric Test Set Optimization of Wafer Probe Data for Predicting in Field Failures and Setting Tighter Test Limits"
Dragoljub (Gagi) Drmanac, Nik Sumikawa, Li-C.Wang, LeRoy Winemberg, and Magdy S. Abadir,
2011 European Design Automation and Test Conference (DATE), March 2011, pages 794-799.

[41] "Wafer Probe Test Cost Reduction of an RF/A Device by Automatic Testset Minimization: A Case Study"
Dragoljub (Gagi) Drmanac, Li-C. Wang, and Michael Laisne,
2011 IEEE International Test Conference (ITC), 10 pages

F. Data Mining for Fmax Prediction, Correlation between Structural Test and Functional Test

[42] "*Predicting multi-core system Fmax by data-learning methodology*"
Janine Chen, Jing Zeng, Li-C. Wang, Michael Mateja, Jeff Rearick,
2010 VLSI Design Automation and Test Symposium, 2010, pages 220-223
(**Nomination for Best Paper**)

[43] "*Correlating system test Fmax with structural test Fmax and process monitoring measurements*"
Janine Chen, Jing Zeng, Li-C. Wang, Michael Mateja,
2010 ACM/IEEE Asia and South Pacific Design Automation Conference, pages 419-424

[44] "*Data learning techniques and methodology for Fmax prediction*"
Li-C. Wang, Janine Chen, Po-Hsien Chang, Jing Zeng, Stanly Yu, and Michael Metaja,
2009 IEEE International Test Conference (ITC), pp. 1-10.

G. Delay Testing With Statistical Learning and Simulation

[45] "*Minimizing Outlier Delay Test Cost in the Presence of Systematic Variability*"
Dragoljub (Gagi) Drmanac, Brendon Bolin, Li-C. Wang, Magdy S. Abadir,
2009 IEEE International Test Conference (ITC), pp. 1-10.

[46] "*A Study of Outlier Analysis Techniques for Delay Testing*"
Sean H. Wu, Dragoljub (Gagi) Drmanac, Li-C. Wang,
2008 IEEE International Test Conference (ITC), pp. 1-10.

[47] "*Statistical Analysis and Optimization of Parametric Delay Test*"
Wu, Sean H.; Lee, Benjamin N.; Wang, Li-C.; Abadir, Magdy S.
2007 IEEE International Test Conference, pp. 1-10.

[48] "*Issues on Test Optimization with Known Good Dies and Known Defective Dies – A Statistical Perspective*"
Benjamin Lee, Li-C. Wang, Magdy S. Abadir,
2006 IEEE International Test Conference (ITC), page 1-10.

[49] "*Hazard-Aware Statistical Timing Simulation and its Application in Screening Frequency-Dependent Defects*"
Benjamin Lee, Hui Li, Li-C. Wang, Magdy S. Abadir,
2005 IEEE International Test Conference (ITC), Austin, Texas, Page(s): 91-100.

[50] "*Reducing Pattern Delay Variations for Screening Frequency-Dependent Defects*"
Benjamin N. Lee, Li-C. Wang, Magdy S. Abadir,
2005 VLSI Test Symposium, May 2005, Page(s): 153-159.

H. Statistical Timing Analysis and Critical Path Selection

[51] "*Refined Statistical Static Timing Analysis Through Leaning Spatial Delay Correlations*"
Benjamin Lee, Li-C. Wang, Magdy S. Abadir,
2006 ACM/IEEE Design Automation Conference (DAC), July, 2006, pp 149-154.

[52] "*Static Statistical Timing Analysis for Latch-based Pipeline Design*"
Mango C-T Chao, Li-C. Wang, Kwang-Ting Cheng, Sandip Kundu,
2004 IEEE/ACM International Conference on Computer-Aided Design, pp. 468 – 472.

[53] "*Critical path selection for delay fault testing based upon a statistical timing model*"
Li-C. Wang, Jing-Jia Liou; K-T Cheng.
2004 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,
Volume 23, Issue 11, Nov. 2004 Page(s):1550 – 1565.

I. Defect-Oriented Testing

[54] "*Defect-Oriented Testing and Defective-Part-Level Prediction*,"
J. Dworak, J.D. Wicker, S. Lee, M.R. Grimaila, M.R. Mercer, K.M. Butler, B. Stewart, and Li-C. Wang,
2001 IEEE Design and Test of Computers, vol 18, no.1, pp. 31-39, Jan/Feb.

[55] "*Defect-Oriented Testing and Defective-Part-Level Prediction*,"
J. Dworak, J.D. Wicker, S. Lee, M.R. Grimaila, M.R. Mercer, K.M. Butler, B. Stewart, and Li-C. Wang,
2001 IEEE Design and Test of Computers, vol 18, no.1, pp. 31-39, Jan/Feb.

[56] "*On the Superiority of DO-RE-ME/MPG-D Over Stuck-at Based Defective Part Level Prediction*,"
J. Dworak, M.R. Grimaila, B. Cobb, T-C Wang, Li-C. Wang, and M.R. Mercer,
2000 Proc. of IEEE Asian Test Symposium, Taipei, Taiwan, pp. 151-157, December.

[57] "*Enhanced DO-RE-ME Based Defect Level Prediction Using Defect Site Aggregation-MPG-D*," J. Dworak, M.R. Grimaila, S. Lee, Li-C. Wang, and M.R. Mercer,
2000 Proc. of the IEEE International Test Conference, Atlantic City, NJ, pp. 930-939

[58] "*Modeling the Probability of Defect Excitation for a Commercial IC with Implications for Stuck-At Fault-Based ATGP Strategies*,"

J. Dworak, M. Grimalia, S. Lee, Li-C. Wang, and R.M. Mercer,
1999 IEEE International Test Conference, Atlantic City, NJ, Sept. 28-30, pp. 1031-1036.

[59] "*REDO-Random Excitation and Deterministic Observation-First Commercial Experiment*,"
M. Grimalia, S. Lee, J. Dworak, K.M. Butler, B. Stewart, H. Balachandran, B. Houchins, V. Mathur, J. Park, Li-C. Wang, and M. Ray Mercer,
1999 IEEE VLSI Test Symposium, Dana Point, CA, April 25-29, pp. 268-274.
(**Best Paper Award**)

[60] "*Using Target Faults to Detect Non-Target Defects*,"
Li-C. Wang, M. Ray Mercer, and Thomas W. Williams,
1996 International Test Conference, Washington D.C., October 20-25, pp. 629-638.

[61] "*On Efficiently and Reliably Achieving Low Defective Part Levels*,"
Li-C. Wang, M. Ray Mercer, and Thomas W. Williams,
1995 International Test Conference, Washington D.C., October 21-25, pp. 616-625.

[62] "*On the Decline of Test Efficiency as Fault Coverage Approaches 100%*,"
Li-C. Wang, M. Ray Mercer, Sophia W. Kao, and Thomas W. Williams,
1995 IEEE VLSI Test Symposium, Princeton, N.J., April 30-May 3, pp. 74-83.

J. Selected Works in PowerPC Array Verification

[63] "*Automatic Generation of Assertions for Formal Verification of PowerPC Microprocessor Arrays Using Symbolic Trajectory Evaluation*,"
Li-C. Wang, Magdy S. Abadir, and Nari Krishnumuthy,
1998 Design Automation Conference, San Francisco, CA, June 15-19, pp. 534-537.

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