ECE 156B - Syllabus

Lecture 0

Description

- In-depth discussion of design process
  - Synthesis (physical sythesis)
  - Two basic algorithms – **SAT** and **OBDD**
  - Verification
  - Timing Analysis
  - Test and Validation
- Lab assignments involve
  - Independent software tools – SAT solver and OBDD package
  - ModelSim and Design Compiler
  - Three assignments (SAT, OBDD, design verification)

Prerequisites

- ECE 156A (required)
  - 156B is a continuation of 156A
- ECE 152A Digital Design Principles
- You should be familiar with the material covered in ECE 152A such as
  - Boolean algebra, switching functions, application of Boolean algebra to the design and analysis of combinational logic nets, minimization procedures, analysis and synthesis of sequential switching circuits, synchronous and asynchronous operation, state minimization, hazards, and races.

Textbooks

- There is really no single book for this course
- *Advanced Digital Design with the Verilog HDL*, by Michael D. Ciletti, Prentice Hall, August 2002
  - You can order online
  - A very comprehensive book
- *Logic Synthesis and Verification Algorithms*, by Gary D. Hachtel and Fabio Somenzi, KAP 1996
  - This is an excellent book to learn about the foundation of synthesis processes

Verilog Tool Options

- We recommend you to use Mentor Graphics Model Sim in the ECI lab
  - Get an account from ECI lab
  - Login from home with X-window display
  - Very handy for experienced user

Design Compiler (ECI)

- We had a tutorial – TA will post it
- Also, the google group for 156B should be created
- TA will send you an e-mail regarding this information shortly

Web Site

- Course web page
  http://mtv.ece.ucsb.edu/courses/ece156B_14/
  - look for an update shortly.
  - The update of course web page usually may be delayed from time to time.
  - Please be patient.

Grading

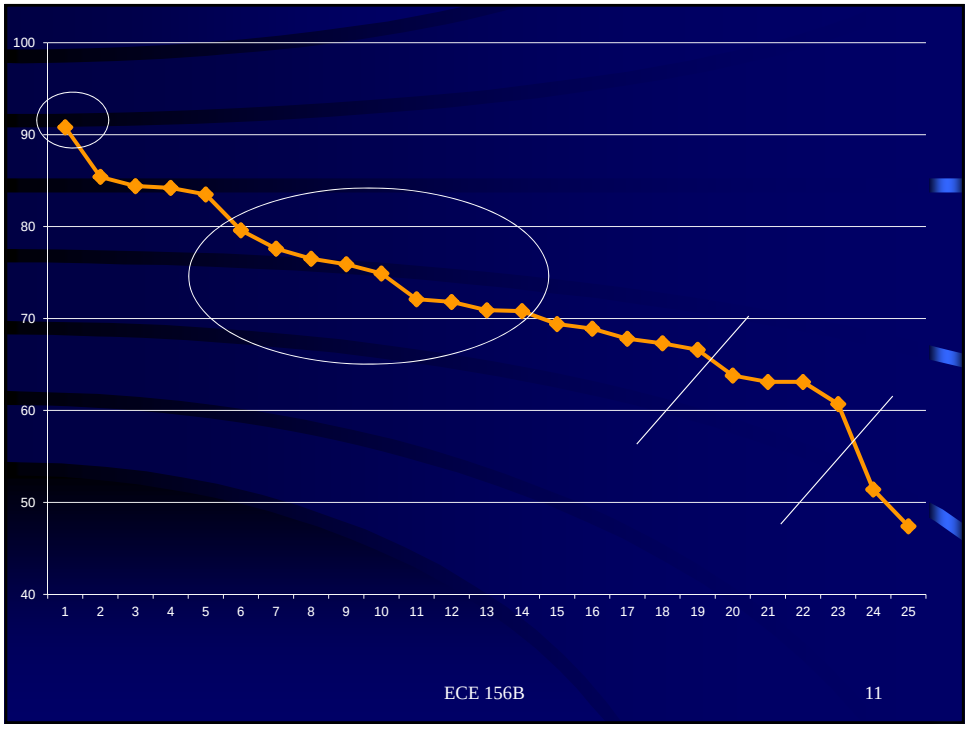
- Homework and Programming Assignments
  - 40%
  - Include a major project
- 2 close-book in-class tests
  - 30% each
  - You must attend the tests at scheduled times
    - We will decide this later
  - **No exception will be made**

TAs

- KK Hsieh
- Office hours:
  - TBD
- We don't usually run the lab session unless it is announced in advance
  - Lab session is TA session

Potential topics covered

- Synthesis of multi-level logic
- Boolean Satisfiability
- Functional representation and binary decision diagram (OBDD)
- Functional verification and equivalence checking
- Timing analysis issues – in depth
- Design for test and scan
- Fault modeling and test generation
- Post-silicon validation
- Diagnosis and debug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