

ACM/IEEE workshop on timing issues in specification and synthesis

Trip summary report

Focus of this year

- Statistical timing analysis techniques
- Is statistical timing the way to go?
- Industrial views on statistical timing
- Cell library modeling – should we continue to use it or abandon it?
- Modeling and characterization
 - Interconnect modeling
 - Waveform model
 - Cross coupling – still an important issue in STA
 - Interconnect-driven physical design (not our interest)

Monday morning

- Keynote speech – The myth of the optimal F04 design, James A. Kahie, IBM corp (director of cell technology)
- Leakage and power – the most concern
 - we are crossing the 50% mark
- Wire dominates delays
 - Buffering is everywhere
- # of latches grow exponentially
 - Merging login into latches
 - Future design will be all latches
 - Hold time analysis will be different
- Process and other variations

How do we know it is too much

- When the design team grows to a few hundred people, we know it is too much
 - We can't do it any more
 - Something has to change
- Future metrics (considered under process variations)
 - Wire-based design
 - Circuit vs. wire balance
 - How well the design will scale
- Limitation of future design
 - # of latches
 - Power and leakage
 - Logic complexity
 - Area increase

Sub 9 – F04 design

- Latches are all that left
 - There are special design techniques merging logic into latches (ISSCC 03 paper?)
 - It will look like L1L2L1L2 ...
 - How do we do timing analysis?
 - So sequential STA makes sense?
- Scan chain design is hard
- Ultimately, latches and wires are everything

Tools

- Variability
 - Process, temperature, power
- Clock skew
- Local temperature (within die analysis)
- Local supply drop
- Better wire model
- Noise analysis
- Optimization vs. analysis
 - Leakage-driven synthesis

Impact on SSTA

- Latch modeling is more important than cell modeling
- We need to consider hold time, clock skew (not necessarily variations, use worst-case bounds first)
- Sequential analysis makes senses
 - We need a new perspective of STA
 - We are analyzing waveforms
 - We need new models and new definition of timing analysis at the abstract level