

**University of California, Santa Barbara**  
**Department of Electrical and Computer Engineering**

**Synthesis and CAD**

**ECE 156B, Winter 2004**  
**TTH 3:30-5pm**

Instructor: Prof. Li-C. Wang  
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Office: Room 3161, Engineering I  
Office Hour: 2-3pm TTH

**Course Organization**

(Continuously Updated)

Course Description: Following the materials in 156A, this course continues to prepare for you to be a logic designer. We will first continue on the chapters left untouched in 156A. This covers most of the synthesis chapters. In this quarter, we will focus on the synthesis tool such as Design Compiler and the synthesis techniques. In the meantime, we will stress on other aspects of design, including *test*, *verification*, and *timing analysis*. I hope to give you a better picture about how today's hardware design flow and design environment may look like.

Prerequisites:

ECE 152A Digital Design Principles --- You should be familiar with the material covered in ECE 152A such as boolean algebra, switching functions, application of Boolean algebra to the design and analysis of combinational logic nets, minimization procedures, analysis and synthesis of sequential switching circuits, synchronous and asynchronous operation, state minimization, hazards, and races.

ECE 156A Logic Design with HDL and Synthesis --- You should have this before.

**Textbook:**

➤ (Required)

*Advanced Digital Design with the Verilog(TM) HDL*, by Michael D. Ciletti

Publisher: Prentice Hall; Book and CD-ROM edition (August 13, 2002) ISBN: 0130891614

➤ (Semi-Required) Logic Synthesis and Verification Algorithms, by Gary D. Hachtel and Fabio Somenzi, KAP 1996

- ✓ This is an excellent book to learn about the foundation of synthesis processes
- ✓ This book cover more advanced topics
- ✓ You may want to have it if you want to be an advance logic designer

Class Web site: Go to my home <http://www.ece.ucsb.edu/Faculty/Wang/default.html> or departmental course web page <http://www.ece.ucsb.edu/courses/syllabi/> and look for an update shortly. The update of course web page usually may be delayed from time to time. Please be patient.

Grading:

Homework and Projects:	50%
In Class Test	20%
Final Exam	30%

Homework: Most assignments will be similar to those in ECE 156A. However, I will need you to go beyond just simulating those designs. You will be asked to (1) synthesize every design into gate-level netlist using design compiler (2) verify that your gate-level netlist is the same as your RTL code using simulation.

Please request an ECI account immediately and setup your DC environment.

In Class Test: In class, **Feb 17, Tuesday**, 1.5 hours closed book exam. Students **MUST** attend this test at the scheduled time.

Final Exam: as scheduled by the university.

Special Announcements:

- ✓ **Feb 16-20**, European Design and Test Conference, Paris, France

TA Information:

Our best guy as always --- Leonard Lee, [lylee@ece.ucsb.edu](mailto:lylee@ece.ucsb.edu)  
Office Hours: M 3-4, W 2-3, F 9-11

Attempted Course Outline:

Week 1: No Lab. Review design methodology.