

ECE 156B - Syllabus

Lecture 0

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Description

- Following the materials in 156A, this course continues to prepare for you to be a logic designer.
- We will first continue on the chapters left untouched in 156A. This covers most of the synthesis chapters.
- In this quarter, we will focus on the synthesis tool such as Design Compiler and the synthesis techniques.
- We will stress on other aspects of design, including
 - *Test and design for testability,*
 - *Verification,* and
 - *Timing analysis.*

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Prerequisites

- ECE 156A
 - You should get at least an A-
- ECE 152A Digital Design Principles
- You should be familiar with the material covered in ECE 152A such as
 - Boolean algebra, switching functions, application of Boolean algebra to the design and analysis of combinational logic nets, minimization procedures, analysis and synthesis of sequential switching circuits, synchronous and asynchronous operation, state minimization, hazards, and races.

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Textbooks

- There is really no single book for this course
- *Advanced Digital Design with the Verilog HDL*, by Michael D. Ciletti, Prentice Hall, August 2002
 - You can order online
 - A very comprehensive book
- *Logic Synthesis and Verification Algorithms*, by Gary D. Hachtel and Fabio Somenzi, KAP 1996
 - This is an excellent book to learn about the foundation of synthesis processes

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Verilog Tool Options

- We recommend you to use Mentor Graphics Model Sim in the EIC lab
 - Get an account from EIC lab
 - Login from home with X-window display
 - Very handy for experienced user
- You can also use the CD software came with the main textbook
 - But it may not be compatible with DC

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Design Compiler (ECI SUN)

- Online documentation
 - /eci/synopsys/sold/sold
- Libraries
 - /eci/synopsys/synthesis/libraries/syn/
 - class.db (basic library)
 - class.sdb (symbol library)
- Executable
 - /eci/synopsys/synthesis/sparcOS5/syn/bin
 - dc_shell
 - design_analyzer
- Tutorial
 - /eci/synopsys/synthesis/doc/syn/tutorial
 - Copy the "tutorial" directory to your home

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Web Site

- Go to my home
<http://www.ece.ucsb.edu/Faculty/Wang/default.html>
- Or departmental course web page
<http://www.ece.ucsb.edu/courses/syllabi/>
 - look for an update shortly.
 - The update of course web page usually may be delayed from time to time.
 - Please be patient.

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Grading

- Homework and Programming Assignments
 - 50%
 - About 6 of them (from 2003 experience)
- Two close-book in-class tests
 - 20% for the 1st test (February 17)
 - 30% for final exam (as scheduled by UCSB)
 - You must attend the tests at scheduled times
 - **No exception will be made**

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Special Schedule

- **February 16-20**, I will not be here
 - TA will teach the class

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TA

- Leonard Lee, lylee@ece.ucsb.edu
- Office hours: Mon 3-4, Wed 2-3, Fri 9-11
- We don't usually run the discussion session unless it is announced in advance
- If we are going to have a discussion session to help you to do the lab, we will have it on Wed
- We will announce discussion session during class

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Intended Course Outline (As of today)

- Week 1: Review of Design Methodology
- Week 2: Continue on synthesis topic
- Week 3: Continue on synthesis topic
- Week 4: Synthesis techniques (combinational)
- Week 5: Synthesis techniques (combinational)
- Week 6: Synthesis techniques (sequential)
- Week 7: Timing analysis
- Week 8: Design for test
- Week 9: Design for test
- Week 10: Verification
- Dead Week: Grade discussion
 - Post-silicon problems

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Potential topics covered

- Synthesis of multi-level logic
- Synthesis of sequential logic
- Functional representation and binary decision diagram
- Timing analysis
- Design for test and scan
- Fault modeling and test generation
- Functional verification and equivalence checking
- Timing validation
- Diagnosis and debug

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