

University of California
Department of Electrical and Computer Engineering
ECE 156B
Synthesis & CAD

Homework 3

DUE: In Class, Thursday, Feb 26

BDD & SAT Exercises

Part a) OBDD (show your steps for getting from the BDD's of the operands to the final answer, arriving magically at the final answer is not satisfactory)

Draw the reduced OBDD for $f = ab$ and $g = bc$

Draw the reduced OBDD for $h = f + g$ (show your work on the left and right sub-trees of f and g)

Draw the reduced OBDD for $i = f \oplus g$ (show your work on the left and right sub-trees of f and g)

Draw the reduced OBDD for $j = hi$ (show your work on the left and right sub-trees of h and i)

Part b) SAT (show all intermediate steps)

Synthesize a 1-bit full adder in Design Compiler. The adder should take 2 1-bit operands a and b , a 1-bit carry in signal cin , and should output the 1-bit sum and 1-bit cout (carryout).

Draw the gate level schematic of the full adder.

XOR sum and cout to a new output, and write the CNF clauses for the circuit that will detect whether a 1 is possible at the output or not.

Generate an input configuration using the CNF formula that will satisfy the output (show intermediate steps you use, such as unit clauses, etc).