

Tutorial Directory:

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/eci/synopsys/2000.11/doc/syn/tutorial
```

Copy this directory to your home directory by doing:

```
cp -r /eci/synopsys/2000.11/doc/syn/tutorial ~
```

Then follow the tutorial. You can find this at

<http://www.eas.asu.edu/~cse518/protected/dctut.pdf> as I couldn't find it in any of the online documentation in the ECI lab. I also mirrored it on

[http://cadlab.ece.ucsb.edu/ece156B\\_04/dctut.pdf](http://cadlab.ece.ucsb.edu/ece156B_04/dctut.pdf) temporarily until the end of the course.

- Chapter 2 is for reference, in case you need any help with the GUI.
- Chapter 5 defines how to set up the environment. Note most of this has already been done.
- Chapter 6 describes the Alarm Clock Design in nitty-gritty detail.
- Start at Chapter 7. Note in this class we will be using the **Verilog** source code (**but be sure to also read the CONVERTER.pla**) instead of VHDL. This chapter shows you how to input your design and various parameters for your design. You can skip the dc\_shell tutorial for now if you want, as it is easier to learn Design Compiler using the GUI. If you want more advanced knowledge of DC later on, you can come back to this tutorial and read about it.
- Continue to Chapter 8. This chapter shows how to set design constraints and debug a warning. Again you can skip the dc\_shell section.
- Continue to Chapter 9: This chapter shows the process of optimizing. **Be sure to output the report on page 258 (9-16) to a file, as you will turn this in. Also output the report on page 267 (9-25) to a file.** You should at least read the part about alternatives to unify to familiarize yourself with the process. Again you can skip the dc\_shell section.
- Continue to Chapter 10: This chapter shows various reports that can be made. **Generate to a file 3 reports of your choosing.** Again you can skip the dc\_shell section.

## Turn in on 1/22/04:

1. Initial report generated at a clock of 25ns.
2. Next report generated at a clock of 23ns.
3. 3 reports of your choosing from Chapter 10.