University of California, Santa Barbara
Department of Electrical and Computer Engineering

Digital Design with HDL and Synthesis

ECE 156A, Fall 2012
MW 5-6:15am

Instructor: Prof. Li-C. Wang
licwang@ece.ucsb.edu
Office hour: Before/after class at HFH 3161 or 2164

Course Organization

Course Description: Introduction to HDL basic elements, HDL simulation concepts, HDL concurrent statements with examples and applications, writing HDL for synthesis, and writing HDL for finite state machines. In this course, we will teach *Verilog* HDL. You will learn the design techniques and methodologies employed in the industry. This course prepares you to be a logic designer.

Prerequisites: ECE 152A Digital Design Principles --- You should be familiar with the material covered in ECE 152A such as boolean algebra, switching functions, application of Boolean algebra to the design and analysis of combinational logic nets, minimization procedures, analysis and synthesis of sequential switching circuits, synchronous and asynchronous operation, state minimization, hazards, and races.

Textbook:

- (Required)

Advanced Digital Design with the Verilog(TM) HDL, 2nd edition by Michael D. Ciletti
Publisher: Prentice Hall; Book and CD-ROM edition (January 2010) ISBN: 0136019285

- (Good Reference) Logic Synthesis and Verification Algorithms, by Gary D. Hachtel and Fabio Somenzi, Springer; (February 10, 2006), ISBN 0387310045
  - ✓ This is an excellent book to learn about the foundation of synthesis processes
  - ✓ This book cover more advanced topics

Class Web site: http://mtv.ece.ucsb.edu/courses/ece156A_11/

Grading:

Homework and Programming Assignments:	40%
Mid term	30%
Final	30%

TA Information:

Nik Sumikawa: nsumikawa@umail.ucsb.edu (Tuesday 4-6pm and Thursday evening Lab)
Brian Neely: bkneely@umail.ucsb.edu (Wed, 8:30-11:30am and Thursday Morning Lab)

Topics Covered and Course Goals:

1. Modern Design Methodologies for Digital Systems
    1. Understand basic design flow
    2. Understand design issues and challenges
    3. Able to use a logic simulator to verify a small design
2. Basic Synthesis Concepts and Logic Minimization
    1. Understand synthesis flow
    2. Comprehend the concepts in 2-level logic minimization
3. Using Verilog to Design Digital Systems
    1. Understand Verilog features and constructs
    2. Able to use structural and behavioral Verilog to model various designs
4. Verilog Synthesis
    1. Understand basic synthesis process and related issues

Laboratory Hours:

3-6 hours per week
About 6-7 Verilog programming assignments for the quarter