Pouria Bastani

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OBJECTIVE

A full-time position, working on a team to push the performance and capabilities of the next-generation products

EDUCATION

M.S./Ph.D. University of California Santa Barbara (Fall 2004 – expected graduation September 2008)
Electrical and Computer Engineering

- Specialization: VLSI
- M.S. grade point average: 3.8/4.0

Ph.D. Research Project (present):

- Researching statistical tools and methodologies for design-silicon correlation
- Investigating issues related to: critical path selection, statistical timing analysis, speed binning, learning of design parameters from silicon test data using machine learning techniques, analyzing the mismatch between predicted timing behavior and actual behavior observed on silicon
- Advisor (and reference): Professor Li-C. Wang
- Sponsored by SRC project ID 1173, 1585

Graduate Level Projects:
VLSI Projects

- Designed, simulated, debugged, Fabricated and tested a SPI slave interface chip in 0.5um CMOS
- Analyzed systematic process variation for sub-micron design
- Implemented full and partial-scan chain testing on a 8-bit RISC microprocessor

Computer Architecture (*in Verilog*)

- Multi-Processor Snoopy Cache: Maintains cache coherency among all processors
- Super Scalar Instruction Dispatch Unit (IDU): Multiple instructions dispatched in one clock cycle

Graduate Level Courses:

- Integrated Systems: VLSI Principles, VLSI Design, Hi-Speed Digital IC Design, Advanced VLSI Design, VLSI Validation, VLSI Testing Techniques, VLSI Design Automation, VLSI Project Design, Mixed Signal Design
- Computer Architecture: Adv. Computer Arch, Sequential Machine and Automata Theory, Distributed Systems

B.S. Saint Louis University, St. Louis, Missouri, May 2004
Parks College of Engineering and Aviation

- Major: Electrical Engineering
- Engineering grade point average: 3.5/4.0 (Dean's List)

WORK EXPERIENCE

Digital Technology Solutions, Strategic CAD Labs Intern
INTEL CORPORATION June 2007 – September 2007 Portland, Oregon

Worked on CAD flow for automating silicon speedpath identification

- Extracted speedpath and non-speed limiting path information for data analysis
- Identified 56 speedpaths on a 65nm Pentium 4 high-performance microprocessor

Analyzed speedpaths to discover dynamic and static root-cause(s) of failure

- Showed that MIS had no impact on 56 speedpaths
- Showed that Cross-coupling noise impacted silicon performance on 20/56 speedpaths
- Showed that localized Di/Dt Voltage droop impacted silicon performance on 15/56 speedpaths

Created a model using Machine Learning (SVM) to predict potential speedpaths

- The model returned a 1% ranked subset of all paths based on similarity to observed speedpaths
- The model predicted 17% of paths that were out of the norm that could potential be speedpaths

Technology Solutions Organization Intern
FREESCALE SEMICONDUCTOR June 2006 – September 2006 Austin, Texas

Project: Apollo 8 Ring Oscillator Statistical Analysis and Validation

- Developed a flow for extraction of channel connected components for custom cells
- Extraction and characterization of ring oscillators using Calibre, StarRXCT and a inhouse characterization tool
- Variance analysis of Silicon measurements and extraction of different components of variation (across chip, chip-to-chip, reticle-to-reticle, wafer-to-wafer, lot-to-lot)
- Silicon validation using deterministic timing with Primetime and statistical static timing analysis (SSTA)
- Analysis of spatial correlation across reticle and across wafer and incorporation to validate the SSTA flow

QCT ASIC Design Intern
QUALCOMM June 2005 – September 2005 San Diego, California

- Profiled the External and AHB Bus interfaces with Burst NOR/PSRAM and SDRAM Memories
- Tested MSM6550 the base band chipset supporting multimedia applications
- Worked with Graphics and Video group to improve ARM926 transaction efficiency

Broadband Group Intern and Electronic Design Automation Intern
ANADIGICS, INC. May – Sept. 2002, 2003 & 2004 Warren, New Jersey

- Tested GaAs wafers for substrate oscillation
- Created and tested a fully automated Test Station for Cable Tuner products and recorded lab measurements
- Tested and debugged circuits together with the Electronic Design Automation Group (EDA)

TEACHING EXPERIENCE

Graduate Teaching Assistant at the University of California Santa Barbara
Synthesis and CAD, HDL and Synthesis Fall & Winter 2005 Santa Barbara, California

- Created, administered and graded homework, exams and class projects
- Provided feedback to students on their homework and class projects

Undergraduate Teaching Assistant at Saint Louis University
Digital Design Winter 2003 St. Louis, Missouri

- Assisted in creating PowerPoint lectures and providing instruction to undergraduate engineering students
- Developed, administered, and graded exams and laboratory projects

COMPUTER AND TECHNICAL SKILLS

- Mentor Graphics ModelSim, Calibre, StarRXCT, Xilinx, Advanced Design Systems (ADS), SUE, MAX, Cadence, Zchaff, PrimeTime, FastScan, DFTAdvisor, FlexTest, Libsvm, LibRF
- Labview, Matlab, Mathmatica, Hspice, Verilog, C-languages, PERL
- Agilent Logic Analyzers and Oscilloscopes

PUBLICATIONS AND CONFERENCES

- P. Bastani, Li-C. Wang, et al. *Analyzing the risk of timing modeling based on path delay test*, ITC 2007
- P. Bastani, L.Wang, et al. *Analyzing the risk of timing modeling based on path delay test*, TECHCON '07 (Best in Session)
- Li-C. Wang, P. Bastani, M. Abadir, *Design-Silicon Timing Correlation: A Data Mining Perspective*, DAC 2007
- P. Bastani, et al. *An Improved Feature Ranking Method for Diagnosis of Systematic Timing Uncertainty*, VLSI-DAT 2008
- P. Bastani, Li-C. Wang, Magady Abadir, *Linking Statistical Learning to Diagnosis – from finding spot defects to identifying systematic uncertainties*, To appear in IEEE Design & Test Special Issue Silicon Debug May/June 2008.
- K. Killpack, A. Krishnamachary, S. Natarajan, C. Kashyap, P. Bastani, *Analysis of Causation of Speed Failures in a Microprocessor: A Case Study*, To appear in IEEE Design & Test Special Issue Silicon Debug May/June 2008
- P. Bastani, et al. *Statistical Diagnosis of Unmodeled Timing Effects*, To appear in DAC 2008 (TAU Workshop 2008)
- P. Bastani, K. Killpack, et al. *Speedpath prediction based on learning from a small set of examples*, To appear in DAC 2008.
- P. Bastani, N. Callegari, Li-C. Wang, M. Abadir, *Diagnosis of design-silicon timing mismatch with feature encoding and importance ranking – the methodology explained*, Submitted to ITC 2008.