

Call For Participation

IEEE 7th International Workshop on Microprocessor Test & Verification (MTV) Hyatt Town Lake Hotel, Austin, Texas, USA December 4-5, 2006

Web Site: <http://mtv.ece.ucsb.edu/MTV/>

Scope

The purpose of MTV'06 is to bring together researchers and practitioners from all areas of work related to verification and test in order to exchange innovative ideas and present new methodologies for solving challenges facing us today in various processor and SoC design environments.

Contacts

General Chair: Magdy S. Abadir, Freescale
(m.abadir@freescale.com)
Program Chair: Li-C. Wang, University of California at Santa Barbara
(licwang@ece.ucsb.edu)
Program Co-chair: Jay Bhadra, Freescale
(jayanta.bhadra@freescale.com)

Advanced Program MTV 2006

Sunday, December 3, 2006

6-8pm: Pre-event Reception and registration at the Hyatt, Town Lake, Austin, TX

Monday, December 4, 2006

7:30-8:30am: Registration and continental breakfast

8:30-9:15am:

Opening Remarks by General Chair

Keynote speech "Selecting A Successful Design Flow Strategy In An Evolving Semiconductor Industry" by Dr. Chekib Akrou, Vice President, Design Technology, Freescale Semiconductor Inc.

9:15-10:30am

Session A: Processor Architecture Compliance
Session Chair: Magdy Abadir (Freescale)

A.1 Using Automatic Detection of Misinterpretations for Validating Processor Architecture Compliance
Allon Adir, Sigal Asaf, Laurent Fournier, Itai Jaeger, Ofer Peled (IBM)

A.2 Verification of the AMBA Protocol
Samin Ishtiaq (ARM)

A.3 IEEE-754/2007: So Many Choices
Dan Zuras (Group70)

10:30am-10:45am: Coffee Break

10:45am – 12:00noon

Session B: Equivalence Checking

Session Chair: Jennifer Dworak (Brown University)

B.1 An Automated Compositional Approach on Sequential Equivalence Checking
In-Ho Moon, Per Bjesse, and Carl Pixley (Synopsys)

B.2 Fast Verification of Complex, but Reasonable, Datapaths
Ted Stanion (Synopsys)

B.3 Transaction Level to RTL Formal Compliance Checking
Carl Pixley (Synopsys)

12noon-1pm: Lunch Break

1pm – 2:15pm

Session C: High Level Test

Session Chair: Vivekananda Vedula (Intel)

C.1 Directed Micro-architectural Test Generation for an Industrial Processor: A Case Study
H.-M. Koo, Prabhat Mishra, Jayanta Bhadra*, Magdy S. Abadir* (University of Florida and *Freescale)

C.2 Software-based on-line test of communication peripherals in processor-based systems for automotive applications
A. Manzone, M. Osella, P. Bernardi*, L. Bolzani*, M. Violante*, M. Sonza Reorda* (Centro Ricerche Fiat and *Politecnico di Torino)

C.3 Circuit Profiling Mechanisms for High-level ATPG
Jorge Campos and Hussain Al-Asaad (University of California at Davis)

2:15 – 2:30pm: Coffee Break

2:30 – 3:45pm

Session D: Verification, and Functional Test Generation

Session Chair: Jayanta Bhadra (Freescale)

D.1 Advanced SAT-Techniques for Bounded Model Checking of Blackbox Designs
Marc Herbstritt, Bernd Becker, and Christoph Scholl (Albert-Ludwigs-University Freiburg)

D.2 A First Look at the Detection of Design Errors Modeled as Missing Logic as a Function of Simulation Vector Quality
Elif Alpaslan and Jennifer Dworak (Brown University)

D.3 MPSoC verification using a unified random program approach
Methodology, tool and case study
Jayaram Nageswaran and Ronald Bos* (University California at Irvine, *Philips Research, Eindhoven)

3:45 – 5:00pm

Session E: Technology Challenges

Session Chair: Kamal Khouri (Freescale)

E.1 Test Implications of in-package/on-chip VRM
T. M. Mak (Intel)

E.2 Statistical Static Timing Analysis Considering The Impact of Power Supply Noise In VLSI Circuits
Hyun Sung Kim and D. M. H. Walker (Texas A&M)

E.3 Fault-tolerant Design in the Era of Variability, Degradation, and Soft Errors
Ming Zhang, T M Mak, Kee Sup Kim (Intel)

5:15 – 10:00pm

Dinner and social event: Best Hill Country Texas BBQ at the Salt Lick Restaurant and Ranch
Bus departs from Hyatt at 5:15pm sharp

Tuesday December 5, 2006

7:45 – 8:30am: Continental Breakfast

8:30am – 10:00am
Session F: Debug and Diagnosis Advances
Session Chair: Al Crouch (Inovys)

F.0 Introduction Modern Debug Issues and Problems (15 mins)
Al Crouch (Inovys)

F.1 Extensible Framework for Semiconductor Debug, Diagnosis and Test
Jason Doege (DA-Test)

F.2 Embedded Compression Diagnosis
Nikhil Dakwala (Stridge)

F.3 Real Fault Insertion for Evaluating Diagnosis Tools
John Potter (Inovys)

10:00am – 10:20am: Coffee Break

10:20am – 12:00pm
Session G: High Level Modeling, Verification and Debug
Session Chair: Jim Holt (Freescale)

G.1 uADL: A Microarchitecture Description and Modeling Tool
Hangsheng Wang, Brian Kahne (Freescale)

G.2 RFSM: A Rendezvous of TLM and RTL
Wei Qin (Boston University)

G.3 Workload Slicing For Characterizing New Features in High Performance Microprocessors
Hassan Al-Sukhni, David Lindberg, James Holt, Michele Reese (Freescale)

G.4 Deep vs. Shallow, Kernel vs. Language – What is Better for Heterogeneous Modeling in SystemC?
Hiren D. Patel and Sandeep K. Shukla (Virginia Tech)

12:00 – 1:00pm: Lunch Break

1:00 – 2:30pm

Panel: Strategies for Convergence Between Design Validation, Test and Debug
Organizers: Vivekananda Vedula (Intel), Jay Bhadra (Freescale)
Moderator: Magdy Abadir (Freescale)

Participants:
Jacob A. Abraham (University of Texas at Austin)
Keith Arnold (Pintail)
Michael Hsiao (Virginia Tech)
Gary Miller (Freescale)
Praveen Parvathala (Intel)
Carl Pixley (Synopsys)
Mick Tegethoff (Cadence)

2:30 – 3:45pm
Session H: Functional Test and Validation
Session Chair: Mark Nodine (Intrinsic)

H.1 *Functional Test Selection for High Volume Manufacturing*
Vijay Gangaram, Deepa Bhan, James K Caldwell (Intel)

H.2 *A Probabilistic Analysis For Fault Detectability of Code Coverage Metrics*
Sreekumar V. Kodakara, Deepak A. Mathaikutty*, Ajit Dingankar**, Sandeep Shukla*, and David Lilja (University of Minnesota, *Virginia Tech and **Intel)

H.3 *Test Calculation for Logic and Delay Faults in Digital Circuits*
József Sziray (Széchenyi University, Hungary)

3:45 – 4:00pm: Coffee Break

4:00pm – 5:15pm
Session I: Error Diagnosis
Session Chair: Alper Sen (Freescale)

I.1 *Abstraction and Refinement Techniques in Automated Design Debugging*
Sean Safarpour, Andreas Veneris (University of Toronto)

I.2 *On Reducing the Global State Graph for Verification of Distributed Computations*
Arindam Chakraborty and Vijay Garg (University of Texas at Austin)

I.3 *Diagnosing Silicon Failures Based on Functional Test Patterns*
C-C. Yen, T. Lin, H. Lin, K. Yang*, T. Liu*, Y.-C. Hsu* (Springsoft Inc. and *Novas Software Inc.)

5:15 – 6:05pm
Session J: Industrial Verification Challenges
Session Chair: Kai Yang (Novas)

J.1 *Embedded Software Validation: Applying Formal Techniques for Coverage and Test Generation*
T. Arons, E. Elster, T. Murphy, E. Singerman (Intel)

J.2 *Challenges in System-on-Chip Verification*
E. Jimenez, E. Chapman, N. Bamford, H. Chavez, L. Lin, R. Dasari, R. Bangalore (Freescale)

6:05pm – Closing Remarks
