
2018
INTERNATIONAL TEST CONFERENCE
October 28 - November 1, 2018
Phoenix Convention Center
Phoenix, Arizona

The 49th International Test Conference (ITC) and the 44th International Symposium for Testing and Failure Analysis (ISTFA) join forces to bring you an even greater experience during your week in Phoenix. There are a couple of things you should know about the co-location before you make your travel arrangements.

The combined ISTFA FA Week and ITC TestWeek™ start on Saturday, October 27, with ISTFA's Educational Short Courses and run through Friday, November 2nd, ending with ITC's workshops. In between, there is much to explore.

Make sure you visit the shared exposition show floor, where you can see more than 120 solution providers in 165 booth spaces eager to present to you the latest tools and equipment for testing, failure and material analysis of semiconductor devices.

Besides the shared exposition show floor, selected sessions are cooperatively organized and are free to join for all registered attendees, so are all keynotes from both conferences, and more. With either conference registration you are invited to attend the following shared program:

- All keynotes
- The ISTFA panel on Tuesday morning
- The ITC plenary session on Tuesday morning
- The diagnosis sessions of ISTFA and ITC, Tuesday and Thursday, respectively
- The ISTFA Hardware Security session on Tuesday, and one the ITC Hardware Security sessions on Wednesday 8:30-10:00
- The ITC and ISTFA poster sessions, both on Wednesday
- The combined Welcome Reception on Tuesday evening
- The show floor with more than 120 solution providers

To attend all technical sessions from both conferences, full-conference attendees in either conference can purchase an add-on ticket for US$350, a substantial discount from the regular registration fee. This add-on ticket can be purchased at the ITC registration booth for ISTFA attendees and at the ISTFA registration booth for ITC attendees. You will also receive the option to download the proceedings of your add-on conference.

If you want to take advantage of additional offerings during your week in Phoenix, not covered by the combination of your registration plus the add-on ticket, please consult the ITC and ISTFA web pages, respectively. There you can register for the ISTFA Educational Short Courses on Saturday, the ITC tutorials on Sunday and Monday, as well as the ITC workshops on Friday. See this PDF for a full grid overview of the entire week.

See you all in Phoenix.

Efrat Moyal
General Chair, ISTFA 2018

Li-C. Wang
General Chair, ITC 2018

ITC Welcome Message

It is our privilege to welcome you to the 49th International Test Conference (ITC) sponsored by IEEE and the IEEE Philadelphia Section. ITC is the world's premier conference dedicated to electronics test. Our volunteer committees worked very hard to provide to you an exciting event with a balance of the latest research, practical applications, and networking opportunities. We are holding ITC 2018 in Phoenix, Arizona, the week of October 28, 2018.

Our topics include emerging test needs for automotive and IoT, hardware security, system test, analog and mixed-signal test, yield learning, test analytics, test methodology, benchmarks, test standards, memory and 3D test, diagnosis, DFT architectures, functional and software-based test. This year we include a special education program with a six-session track of invited talks on various topics of AI. We also have two additional devoted tracks: The Security Track with papers, special sessions and a keynote address; and the Automotive Track, with a similar format, that leads into the Automotive Test Workshop which immediately follows the conference.

In addition to the usual best paper award, we have selected several papers based on reviewers' scores to be Distinguished Papers. These outstanding papers will be identified in the program.

ITC has expanded its presence! For the second year, in 2018 there are ITC-Asia and ITC-India conferences in China and Bangalore, respectively. We are pleased to include the best papers of those conferences in our program this year.

The conference is organized in a way to provide you various methods to learn and discuss topics related to electronics test. Our keynote speakers are well known industry leaders and academic researchers that provide exciting insights. The technical papers are 25-minute presentations of papers that were selected from a rigorous review process—with a few minutes for questions at the end of each paper.

The exhibition floor consists of solutions providers who are available for discussion and learning about their offerings. A corporate forum is held on the exhibit floor where exhibiting companies present about their products. This year we have one poster session held on the exhibition floor. Posters provide a very comfortable and informal environment to discuss details with the authors.

We recognize that networking is extremely valuable to our attendees. Multiple breaks and social events are integrated in the program to allow you to network with colleagues and other specialists. Free lunches are provided in the exhibit hall for full- and one-day ITC conference attendees.

On behalf of the 2018 International Test Conference steering committee, program committee and all the dedicated volunteers who are key to making the program complete, we welcome you to this year's exciting technical program and exhibits.

Li-C Wang
General Chair

William Eklow
Program Chair

Sponsors

IEEE

IEEE Philadelphia Section

Corporate Supporters

Diamond

Mentor A Siemens Business

Platinum

ADVANTEST

Silver

ASTRONICS TEST SYSTEMS

cadence

Bronze

pickering

SYNOPSYS

ITC Test Week Highlights

	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday
12 Half-Day TTTC Tutorials A great way to prepare for the ITC Technical program	●	●				
Four Panels		●	●		●	
Plenary Session and Keynotes			●	●	●	
76 Technical Presentations		●	●	●	●	
Three Tracks: AI, Security and Automotive			●	●	●	
Six Special Sessions			●	●	●	
World-Class Exhibits Free admission to exhibits floor on all days			●	●	●	
Exhibits Passport Program Visit booths and be eligible for a prize			●	●	●	
Corporate Forum The latest technical innovations from our exhibitors and corporate supporters			●	●		
37 Posters				●		
TwoEmbedded Tutorials Included within the technical paper sessions				●	●	
Two-Day Workshops Three to choose from					●	●
ITC Receptions		●	●			
Fringe Technical Meetings	●	●	●	●	●	●

Become an ITC corporate supporter or utilize marketing opportunities

http://www.itctestweek.org

Follow Us On twitter

www.twitter.com/itctestweek

Test Week At-a-Glance

SUNDAY, OCTOBER 28 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial1 Learning Techniques for Reliability Monitoring, Mitigation Adaptation	Tutorial 2 Integrated Bulk Sensors enabling Online Test for Radiation-induced Soft-Errors and Noise Sensing	Tutorial 3 Targeting "Zero Defect" IC Quality: Advanced Cell-aware Fault Models and Adaptive Test Automotive Reliability and Test Strategies
1:00 p.m. – 4:30 p.m.	Tutorial 4 Machine Learning for Test and Test for Machine Learning	Tutorial 5 Mixed-Signal DFT and BIST: Trends, Principles and Solutions	Tutorial 6 Beyond DFT: The Convergence of DFM, Variability, Yield, Test, Diagnosis and Reliability

MONDAY, OCTOBER 29 – HALF-DAY TUTORIALS			
8:30 a.m. – 12:00 p.m.	Tutorial 7 Memory Test and Repair in the FinFET Era	Tutorial 8 From Data to Actions: Application of Data Analytics in Semiconductor Manufacturing and Test	Tutorial 9 High-Speed I/O Testing in High-Volume Manufacturing
1:00 p.m. – 4:30 p.m.	Tutorial10 Automotive Reliability and Test Strategies	Tutorial 11 Testing of TSV-based 2.5D- and 3D-Stacked ICs	Tutorial12 Test to Post-Silicon Validation: Concepts and Recent Trends

MONDAY, OCTOBER 29 – PANEL	
4:45 p.m. –6:15 p.m.	Panel 1 *Physical Inspection and Attacks: New frontiers in Hardware Security*

MONDAY, OCTOBER 29 – POST-PANEL RECEPTION	
6:15 p.m. –8:00 p.m.	Post-Panel Reception/Social

TUESDAY, OCTOBER 30 – TECHNICAL SESSIONS					
9:00 a.m. – 10:30 a.m.	Plenary – Keynote Address *Working with Safe, Deterministic and Secure Intelligence from Cloud to Edge* Kenneth P. Caviasca				
10:30 a.m. – 5:30 p.m.	Exhibits - Shared with ISFTA				
12:00 p.m. – 1:30 p.m.	Corporate Forum				
11:30 p.m. – 1:30 p.m.	Lunch				
1:30 p.m. – 3:30 p.m.	Session 1 Test Cost Reduction	Session 2 Optimization and Simulation	Session 3 New Advances Related to Memories	IEEE TTTC E. J. McCluskey Best Doctoral Thesis Award: Final Competition	AI 1 Safe and Unbiased AI
4:00 p.m. – 5:30p.m.	ITC Asia 2018 Top Three Papers	Special Session 1 New IEEE Standardization Efforts	Security 1 Security Track Special Session: Analog Circuit Security	Poster Highlights Presentations of Top 10 Posters	AI 2 Robust and Accountable AI

TUESDAY, OCTOBER 30 – WELCOME RECEPTION	
5:30 p.m. –7:15 p.m.	ITC and ISFTA Joint Welcome Reception

Security Track **Automotive Track** **AI Track**

Test Week At-a-Glance

WEDNESDAY, OCTOBER 31 – TECHNICAL SESSIONS					
8:30 a.m.–10:00 a.m.	Session 4 Analog and Asynchronous	Session 5 3D test	Session 6 Security Track: Hardware Trojans	Special Session 2 Embedded Tutorial: Analog Fault Simulation	AI 3 Machine Learning in Yield Learning
9:30 a.m.–4:30 p.m.	Exhibits - Shared with ISFTA				
10:30a.m.–12:00 p.m.	Special Session 3 Testing of Gigascale Designs	Session 7 Advanced and Emerging Devices	Session 8 Security Track: Securing Hardware and DFT	Automotive 1 Case Studies of Automotive SOCs	Session 9 Machine Learning in Test and Diagnosis
12:00 p.m.–2:00p.m.	Poster Session - Lunch				
12:00 p.m.–2:00p.m.	Corporate Forum				
2:00 p.m.–3:30 p.m.	ITC India 2018 TopThree Papers		Session 10 Security Track: Trust but Verify	Automotive 2 Panel: Automotive Functional Safety: How Much Is Enough?	AI 4 AI and Autonomous Machines
4:00 p.m.–5:00 p.m.	Keynote Address *Trick or Treat: Is Your Supply Safe?* Matthew Casto				

THURSDAY, NOVEMBER 1– TECHNICAL SESSIONS					
9:00 a.m.–10:30 a.m.	Session 11 Novel Diagnosis Approaches	Session 12 Communication and Interface Testing	Special Session 5 Beyond System Test	Session 13 Analog Safety and BIST for Automotive	AI 5 AI-enabled ATE
9:30 a.m. – 1:30 p.m.	Exhibits				
11:00 a.m.–12:00 p.m.	Mini-Keynote Session Elevator Talks on Different Perspectives of AI				
12:00 p.m.– 1:30 p.m.	Lunch				
1:30 p.m.– 3:00 p.m.	Special Session 6 Advanced Memory	Special Panel ITC 50—Remember the Past and Imagine the Future		Automotive 3 Embedded Tutorial: Automotive Reliability	AI Panel Could AI Eliminate the Need for Test Engineering?

THURSDAY, NOVEMBER 1 – WORKSHOPS			
4:00 p.m. – 4:30 p.m.	Opening Address		
4:30 p.m. – 6:30 p.m.	Automotive Reliability and Test	Test and Validation of High-Speed Analog Circuits	Silicon Photonics Design and Test
7:00 p.m. – 9:00 p.m.	Workshop Reception		

FRIDAY, NOVEMBER 2 – WORKSHOPS			
8:00 a.m. – 4:00 p.m.	Automotive Reliability and Test	Test and Validation of High-Speed Analog Circuits	Silicon Photonics Design and Test

Security Track **Automotive Track** **AI Track**

TTTC TEST TECHNOLOGY EDUCATION PROGRAM (TTEP) 2018

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes a comprehensive set of Test Technology Tutorials to be held in conjunction with several TTTC-sponsored technical meetings worldwide. The mission of the Test Technology Educational Program (TTEP) is to serve test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics. TTEP offers tutorial participants the opportunity to earn official certification from IEEE Computer Society TTTC. Each half-day tutorial corresponds to two TTEP units. Upon completion of 16 TTEP units, official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to the participant. For further information regarding TTEP, please visit http://ttep.tttc-events.org/ttep/index.html

At ITC 2018, TTTC/TTEP is pleased to present 12 **half-day tutorials** on topics of current interest to test professionals and researchers. All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Six tutorials are held on Sunday, October 28. Six tutorials will be held on Monday, October 29.
The **one-day** tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
The **all-access pass** tutorial registration provides in-and-out access to all twelve tutorials over both days.
(see registration page or http://www.itctestweek.org for further information). Admission for onsite registrants is subject to availability.

Tutorial attendees receive study material, breaks and lunches on the days attended. Tutorial registration, coffee and pastry are available at 7:00 a.m. on Sunday and Monday.

Sunday 8:30 a.m. – 12:00 p.m.

TUTORIAL 1
Learning Techniques for Reliability Monitoring, Mitigation Adaptation

Presenter M. Tahoori

With increasing complexity of digital systems and the use of advanced nanoscale technology nodes, various process and runtime variabilities threaten the correct operation of these systems. The interdependence of these reliability detractors and their dependencies to circuit structure as well as running workloads makes it very hard to derive simple deterministic models to analyze and target them. As a result, machine learning techniques can be used to extract useful information which can be used to effectively monitor and improve the reliability of digital systems. These learning schemes are typically performed offline on large data sets in order to obtain various regression models which then are used during runtime operation to predict the health of the system and guide appropriate adaptation and countermeasure schemes.

TUTORIAL 2
Integrated Bulk Sensors enabling Online Test for Radiation-induced Soft-Errors and Noise Sensing

Presenters F.Torres, R. Bastos

Integrated bulk current sensors offer a promising solution for detection of radiation-induced transient faults and soft errors, substrate noise analysis, and detection of maliciously induced transient effects on secure circuits. Consequently, these bulk built-In current sensors (BBICS) are of interest for online testing as well as diagnosis purposes that explore the design's safety and reliability. The main objectives of this tutorial are the presentation of the main concepts of integrated bulk current sensors, the discussion of design methods, and the introduction of strategies for system integration. Further aspects are a thorough analysis of radiation-induced effects in current technologies, sensor testing methods, and the exploration of its applicability for on-chip noise sensing

TUTORIAL 3
Targeting "Zero Defect" IC Quality: Advanced Cell-aware Fault Models and Adaptive Test Automotive Reliability and Test Strategies

Presenter A. Singh

Commercial applications continue to demand ever-higher IC quality. Meanwhile, recent experience with new fault models suggests that current structural test methodologies can miss significant defectivity, resulting in increasing reliance on expensive system-level tests as a final defect screen. This two-part tutorial presents a comprehensive study of known state-of-the-art techniques directed at targeting "Zero-Defect" IC quality. Part one focuses on new fault models, including the cell-aware methodology, for an in-depth understanding of the actual defects in modern standard cells that are missed by conventional stuck-at and TDF tests but detected by the new fault models. Part two presents adaptive test methods that employ innovative statistical techniques to further improve test effectiveness by optimizing the tests applied to individual parts.

TTTC Half-Day Tutorials

Sunday 1:00 p.m. – 4:30 p.m.

TUTORIAL 4
Machine Learning for Test and Test for Machine Learning

Presenter L-C. Wang

Applying "machine learning" (ML) in design and test has received growing interests in recent years. Many potential applications have been demonstrated and tried. In this tutorial, I will begin with a review of the basic principles for applying ML in selected applications and highlights key barriers for deploying a ML-based solution, including data barrier, theoretical barrier, computational barrier, and barrier in competing with an existing solution. Results based on actual industrial settings will be used to explain a development journey toward building an AI system which can be called Intelligent Engineering Assistant (IEA). I will explain what "engineering intelligence" means in such a system in terms of some selected applications. In principle IEA is similar to other AI systems such as autonomous vehicles and consequently, the deployment of an IEA system will face a set of test and verification questions regarding the ML components employed.

TUTORIAL 5
Mixed-Signal DFT and BIST: Trends, Principles and Solutions

Presenter S. Sunter

The lack of systematic analog DFT explains why analog accounts for the majority of failures in automotive mixed-signal ICs. We'll try to improve this situation. We first review trends in ad hoc DFT and fault simulation, IEEE 1149.1/4/6/7/8/10, and 1687, and ISO 26262, continuing on to BIST for ADC/DAC, PLL, SerDes/DDR, and random analog. Next, essential principles of practical analog BIST are presented including, for instance, addition, subtraction, and spec-based defect-oriented test, followed by practical DFT techniques, ranging from quicker analog fault coverage simulation to over/under sampling methods that greatly improve range, resolution, and reusability. We conclude with the two analog test coverage and access standards being developed by engineers from 30 companies, and measurement of related ISO 26262 metrics.

TUTORIAL 6
Beyond DFT: The Convergence of DFM, Variability, Yield, Test, Diagnosis and Reliability

Presenters S. Venkataraman, R. Aitken

The tutorial shows how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. DFM techniques to analyze design content, flag potential yield limiters, and make changes are discussed. Test techniques close the loop by exposing the defect prone feature and circuit marginality through ATPG, and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it.

TTTC Half-Day Tutorials

Monday 8:30 a.m. – 12:00 p.m.

TUTORIAL 7
Memory Test and Repair in the FinFET Era

Presenter Y. Zorian

Recent growth in content delivery has led to an explosion in the use of embedded memories. This tutorial will present the trends and challenges of growing memory content on chip and how to ensure detection of today's defects upon manufacturing and during life time, including process variation and FinFET-specific defects including 7-nm technology. BIST and repair solutions to address debug, diagnosis, yield optimization and data retention of failure modes will be presented. Given the tens of thousands of embedded memory instances in today's SOCs, this tutorial will also cover power management constraints, functional timing implications, test scheduling optimization, and area minimization options.

TUTORIAL 8
From Data to Actions: Application of Data Analytics in Semiconductor Manufacturing and Test

Presenters Y. Makris, H. Stratigopolos

Throughout the lifetime of an integrated circuit, a wealth of data is collected for ensuring its reliable operation. Ranging from design-time simulations to process characterization monitors and from high-volume specification tests to diagnostic measurements on customer returns, the information inherent in this data is invaluable. At the same time, cost-effective test solutions are urgently needed, especially in complex mixed-signal SoCs. As a result, using data analytics methods to mine this information and identify meaningful correlations has seen intense interest and numerous breakthroughs during the last decade. This tutorial seeks to elucidate the utility of data analytics in semiconductor manufacturing and test. Relevant concepts from data analytics will be introduced, agglomerated with current practice, and showcased using industrial data.

TUTORIAL 9
High-Speed I/O Testing in High-Volume Manufacturing

Presenters S. Abdennadher, S. Shaik

With advances in VLSI technology, packaging and architecture, Systems-on-Chip (SoC) continue to increase in complexity. Increasing complexity has resulted in an unprecedented increase in design errors, manufacturing flaws and customer returns related to high-speed I/O (HSIO) circuits. This tutorial presents challenges and existing techniques to meet test complexity of HSIO and methodologies needed to achieve the high-quality usually mandated by the critical applications such as automotive and medical, etc. Both the system and block-level test techniques with particular emphasis on DFT/BIST-based methods and their suitability to production-level environment are presented in this tutorial. Additionally, this tutorial includes a section on test practices for 2.5D/3D products with IO interfaces.

Monday 1:00 p.m. – 4:30 p.m.

TUTORIAL 10
Automotive Reliability and Test Strategies

Presenters R. Mariani, Y. Zorian

Given today's fast growing automotive semiconductor industry, this tutorial will discuss the implications of automotive test, reliability and functional safety requirements on all aspects of the SOC lifecycle. This will include design, silicon bring-up, volume production, and particularly in-system test stages. Today's automotive safety-critical chips need multiple in-system self-test modes, such as power-on self-test and repair, periodic in-field self-test, advanced error correction solutions, etc. This tutorial will analyze these specific in-system test modes and the discuss the benefits of selecting ISO 26262-certified solutions, in order to ensure that standardized functional safety requirements are met, while accelerating time to market for automotive SOCs.

.

TUTORIAL 11
Testing of TSV-based 2.5D- and 3D-Stacked ICs

Presenter E. J. Marinissen, K. Chakrabarty

After a long period of technology hype, finally real 3D-stacked ICs containing through-silicon vias and microbumps (and also their interposer-based 2.5D-SIC variant) are hitting the market. Testing of 2.5D- and 3D-SICs is fraught with new test and design-for-test challenges, for which solutions are only emerging. The test challenges are the following. (1) Test flows: what to test for when? (2) Test content: do these stacked ICs bring new defects and faults and how do we test for those? (3) Test access: how do we pump in/out the test stimuli/responses into the dies and die stacks? In this tutorial, we present test flow cost modeling and optimization, advances in 3D probe technology, advanced 3D-DfT architectures and optimization, and the latest details of the ongoing IEEE Std P1838 standardization effort for test access

TUTORIAL 12
Test to Post-Silicon Validation: Concepts and Recent Trends

Presenters A. Sinha, S. Ray

The tutorial will provide a comprehensive overview of post-silicon validation, from readiness and planning to execution. The diverse activities involved in enabling the validation on modern system-on-chip design at various phases of the system life-cycle will be covered, and the conflicts, cooperation, and trade-offs will be discussed. The trade-offs span a vast spectrum of activities, including security, power management, and physical design, and we will provide an overview of its complexity as well as industrial best practices. We will describe how we can leverage of the design for test infrastructure for post-silicon validation, and the collaboration areas between validation and test. We will cover several instrumentation, control, and observability technologies including tracing and triggering, scan dumping, and off-chip transport mechanisms.

Exhibits

Exhibits hours: Tuesday 10:30 a.m. – 5:30 p.m.
Wednesday 9:30 a.m. – 4:30 p.m., Thursday 9:30 a.m. – 1:30 p.m.
The ISFTA exhibition on Tuesday and Wednesday is open to all registered ITC attendees.

FREE ADMISSION TO EXHIBITS

ITC is offering free exhibits-only registration to visit the exhibit hall during all exhibit hours. Onsite registration for this special opportunity begins on Tuesday at the ITC registration area in the Phoenix Convention Center North Hall, third floor. Lunch is not included with free exhibits-only admission.

ITC Exhibitors*

Advantest
Aehr Test Systems, Inc.
Alliance ATE Consulting Group, Inc.
Aries Electronics, Inc.
Astronics Test Systems
Chroma ATE, Inc.
Cohu
EDA Industries
ELES Semiconductor Equipment Spa
Evaluation Engineering
Exatron
GOEPEL Electronics LLC
HSIO Technologies
INNO GLOBAL
Integrated Test Corp.
Ironwood Electronics
Marvin Test Solutions, Inc.
Mentor, A Siemens Business
Micro Control Company
MJS Designs
NHK
PDF Solutions, Inc.
Pickering Switching Solutions
Qualtera
R&D Altanova
Ridgetop Group, Inc.
Roos Instruments
Sensata Technologies
SiliconAid Solutions
Synopsys, Inc.
TDK-Lamda Americas
Teradyne
TESEC, Inc.
Test Spectrum
Textron Systems
TSSI
TTTC

** As of publication date*

ISTFA Exhibitors*

Advanced Spectral Technology, Inc.
Allied High Tech Products
Angstrom Scientific, Inc.
Anton Paar
Applied Beams
Attolight AG
Barnett Technical Services
Bruker AXS INC.
BSET EQ
Buehler, An ITW Company
Checkpoint Technologies
Contech Solutions Inc.
Control Laser Corp
DC - Digit Concept
EAG Laboratories
EDAX Inc.
Electron Microscopy Sciences
Ephemeron Labs Inc
FLIR Systems, Inc
Gallant Precision Machining Co., Ltd
Gatan
Hamamatsu Corporation
HDI Solutions - Hitachi
Herzan LLC
Hi-Rel Laboratories
Hitachi High Technologies
ibss Group
Imina Technologies SA
IR Labs
JEOL USA
JIACO Instruments
Keyence Corporation
Kleindiek Nanotechnik
LatticeGear
Leica Microsystems
MASER Engineering B.V.
Materials Analysis Technology
Mentor, A Siemens Business
Mesoscope Technology Co. Ltd.
Micromanipulator
MicroNet Solutions, Inc.
Microsanj LLC
Microtech Laboratories
MSSCORPS Co., Ltd.
Nanoscience Instruments
Nanotronics
Neocera LLC
Nikon Metrology
Nippon Scientific Co., Ltd.
Nisene Technology Group, Inc.
Nordson Dage / Nordson Sonoscan
OKOS
Olympus
Oxford Instruments
PACE Technologies
Park Systems Inc.
PrimeNano Inc.
PVA TePla America Inc.
Quantum Focus Instruments
Quartz Imaging
Raith America, Inc.
RKD Engineering
RKD Systems
Robson Technologies Inc.
Rolink, LLC
Sage Analytical Lab
Samco Inc.
SELA USA Inc.
SEMICAPS
SmarAct Inc
SPI Supplies, Inc.
Synopsys
Ted Pella
TeraView LTD
TESCAN USA
Thermo Fisher Scientific
TMC Ametek
Trion Technology
ULTRA TEC
Varioscale Inc.
XEI Scientific
Yxlon FeinFocus
ZEISS
Zurich Instruments AG

** As of publication date*

Corporate Forum

The Corporate Forum track will be on Tuesday and Wednesday. Except for our Diamond Supporter presentation, it will take place in a comfortable meeting area adjacent to the exhibits floor. This will make it easier for ITC exhibit attendees to drop in to see forum presentations. It provides our exhibitors and supporters an opportunity to present the latest developments from their companies, and to promote their activities at ITC.

Our Diamond Supporter, Mentor, A Siemens Business, will provide a one-hour presentation on Tuesday morning at 10:45 a.m. in room 120D. The remaining presentations in the exhibit hall will start at 12:00 p.m. at 20-minute intervals, spread across Tuesday and Wednesday to minimize conflict with the conference technical program. The 20-minute length allows attendees to enjoy multiple presentations in a short time span and runs at a fast pace to keep this event more interesting. Check back for complete presentation schedule.

R. Knoth, Chair

Tuesday 10:45 a.m.–11:45 a.m.

10:45 a.m. Diamond Supporter Session
Mentor, A Siemens Business
Test for the Autonomous Age with Customer Success

Tuesday 12:00 p.m.–1:30 p.m.

12:00 p.m. Marvin Test
Cost-effective Metal-Oxide (MOX) Gas Sensor Testing

12:20 p.m. GOEPEL Electronics
Next-Generation Embedded JTAG Solutions: Synthetic Instruments

12:40 p.m. Advantest
` Pattern- and Test-Sequence-Synchronized Temperature and Power Measurement for Improved Yield, Performance Optimization and Equipment Investigations

1:00 p.m. Cadence
Diagnostics - Just What The Doctor Ordered

Wednesday 12:00 p.m. – 2:00 p.m.

1:00 p.m. Synopsys
Maximizing Automotive Quality and Functional Safety with Synopsys Test Solutions

Plenary & Keynote Address

Tuesday 9:00 a.m. – 10:30 a.m.

Opening Remarks
Li-C Wang, *ITC 2018 General Chair*

ITC 2018 Program Introduction
William Eklow, *ITC 2018 Program Chair*

ITC 2017 Paper Awards Presentation
Peter Maxwell, *ITC 2017 Program Chair*

TTTC Awards Presentation
Yervant Zorian, *TTTC President*

Keynote Address

Working with Safe, Deterministic and Secure Intelligence from Cloud to Edge

Kenneth P. Caviasca *Vice President, Internet of Things Group, General Manager, Architecture, Silicon and Platform Engineering, Intel*

The Internet of Things (IoT) will be the largest revolution in the data economy. At Intel, we understand the exponential power of data, and we're making it practical and economical to put it to work from the edge to the cloud. Intel® technologies purpose-built for IoT deliver optimized performance at every point, practical ways to use artificial intelligence, broad connectivity support, and a built-in foundation of security to help protect your data and systems. Proven solutions from our partner ecosystem can reduce the time, cost, and risk of IoT deployments. By harnessing the massive flood of data generated by connected things—and using it to gain actionable insights—we'll accelerate business transformation to a degree never seen before.

About the speaker Kenneth P. Caviasca is vice president in the Internet of Things Group and general manager of architecture, silicon and platform engineering at Intel Corporation. He has overall responsibility for computing platforms targeted to the Internet of Things (IoT) market segment, including planning, architecture, user experience priorities, silicon definition, operating system porting, hardware, firmware, validation and manufacturing test. Between 2008 and 2010, Caviasca's development team won several premier supplier awards from industry-leading communications equipment suppliers. He and his team also won an Intel Achievement Award in 2004 for excellence in network processor development. Caviasca earned his bachelor's degree in computer and electrical engineering from the University of Bridgeport in Connecticut and his MBA degree from the W. P. Carey School of Business at Arizona State University. He holds seven patents in circuits, CPU and video systems architecture.

Wednesday ITC Keynote

4:00 p.m. – 5:00 p.m.

Trick or Treat: Is Your Supply Safe?

Matthew Casto *Chief, Trusted Electronics, Air Force Research Laboratory*

Much like candy that ends up on the kitchen table at the end of a successful Halloween night, the microelectronics supply chain is a diverse bag of goodies that needs to be checked before it can be consumed. This talk will explore challenges and opportunities in trusting and assuring an increasingly complex electronics global supply chain.

About the speaker Dr. Matthew Casto is chief of the Air Force Research Laboratory, Sensor's Directorate, Trusted Electronics Branch and is the Air Force's Hardware Assurance technical lead for the Department of Defense (DoD) Joint Federated Assurance Center. Dr. Casto is a Senior Electronics Engineer with a BSEE and MSEE degree from Wright State University, and a PhD from The Ohio State University Electro-science Laboratory. In his current role, Dr. Casto leads the Science and Technology portfolio for the DoD's Trusted and Assured Microelectronics Initiative, developing a new trust approach to ensure enduring availability and assured access to state-of-the-art microelectronics.

Thursday ITC Keynotes

11:00 a.m. – 12:00 p.m.

Mini-Keynotes: Elevator Talks on Different Perspectives of AI

Instead of a regular keynote, this plenary session comprises several elevator talks to provide different perspectives on AI in test. A follow-up panel will be held in the afternoon for further discussion.
The speakers include:

Ken Butler, *Texas Instruments* Semiconductor Test Perspective
Anne E Gattiker, *IBM* Deep Learning Perspective
Ira Leventhal, *Advantest* ATE Perspective
Xinli Gu, *Huawei* System Perspective
Cheng-Wen Wu, *NTHU, Taiwan* AI on Taiwan Semiconductor Industry

ISTFA Keynotes

Wednesday, 10:05 a.m.–11:35 a.m.

Hardware Root-of-Trust for Cyber Security: Uncovering the Role of Test and Failure Analysis in Enabling Cyber Defense
Mark Tehranipoor, *University of Florida*

Transformation to Automated Driving
Mark-Tami Hotta, *Integrity First Consulting Services LLC*

2:00 p.m. – 4:00 p.m.

SESSION 1
Test Cost Reduction

1.1 Fine-Grained Adaptive Testing Based on Quality Prediction

1.2 Access-Time Minimization in the IEEE 1687 Network Using Broadcast and Hardware Parallelism

1.3 Hypercompression of Test Patterns

1.4 Total Critical Area Based Testing

SESSION 2
Optimization and Simulation

2.1 Analysis of Production Tests Coverage in the Simulation Environment

2.2 On Close-to-Functional Test Sequences

2.3 Improving Power, Performance and Area with Test: A Case Study

2.4 Optimizing the Use of Simulations for Commissioning with Systems Engineering Principles and Objective Analysis

SESSION 3
New Advancements Related To Memories

3.1 Test of Supply Noise and Endurance for Emerging Non-Volatile Memories

3.2 Electrical Modeling of STT-MRAM Defects

3.3 An Effective Intra-Cell Diagnosis Flow for Industrial SRAMs

3.4☆ Fault Tolerance for RRAM-Based Matrix Operations

Click here to see session chairs and presenters.

IEEE TTTC E. J. McCLUSKEY BEST DOCTORAL THESIS AWARD: FINAL COMPETITION

PhD 1 Towards Provably Secure Logic Locking for Hardening Hardware Security

PhD 2 On New Class of Test Points and Their Applications

PhD 3 Transmitter and Receiver Equalizers Optimization Methodologies for High-Speed Links in Industrial Computer Platforms Post-Silicon Validation

PhD 4 Variation-aware Hardware Trojan Detection through Power Side-Channel

SESSION AI1
Safe and Unbiased AI

AI 1.1 Introduction To AI Theme in ITC 2018

AI 1.2 Safe AI in CPS

AI 1.3 The Mismeasure of AI

4:00 p.m. – 5:30 p.m.

ITC ASIA SESSION
Top Three Papers From ITC Asia 2018

ITC-Asia 1 Generating Compact Test Patterns for DC and AC Faults Using One ATPG Run

ITC-Asia 2 Lightweight Timing Channel Protection for Shared DRAM Controller

ITC-Asia 3 A New Technique to Generate Test Sequences for Reconfigurable Scan Networks

SPECIAL SESSION 1
IEEE Standardization Efforts

S1.1 Towards an Analog Fault Standard

S1.2 Extending 1687 to Low Pin- Count and Mixed-Signal ICs

S1.3 STAM: The Final Frontiers of System Test Access Management

SECURITY 1
Security Track Special Session: Analog Circuit Security

SEC 1.1 Using RF Front-End Characteristics for Supply Chain Tracking and Counterfeit Detection

SEC 1.2 Securing Mixed-Signal ICs via Logic Locking

SEC 1.3 Process-specific Functions for Assurance of Analog Mixed-Signal Integrated Circuits

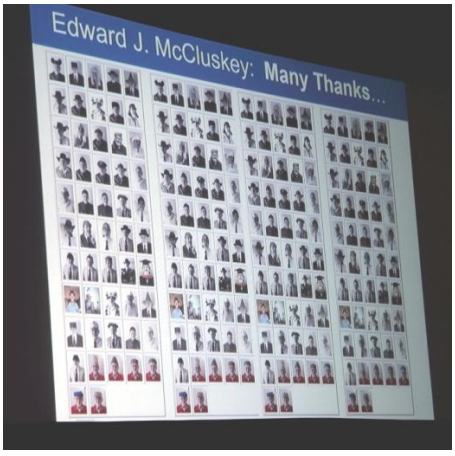
POSTER HIGHLIGHTS
Presentation of Top Ten Posters

Click here to see posters with Top 10 indicated §.

SESSION AI 2
Robust and Accountable AI

AI 2.1 Seeing Faces Through the Eyes of Artificial Intelligence

AI 2.2 Influence-directed Explanations for Machine Learning Systems



Wednesday Morning

8:30 a.m. – 10:00 a.m.

SESSION 4
Analog and Asynchronous

4.1 On the use of Bayesian Networks for Resource-Efficient Self-Calibration of Analog/RF ICs

4.2 Test methodology for PCHB/PCFB based asynchronous pipeline circuits

4.3 ☆ Fast and accurate linearity test for DACs with various architectures using segmented models

SESSION 5
3D Test

5.1☆ Solutions to Multiple Probing Challenges for Test Access to Multi-Die Stacked Integrated Circuits

5.2 On-Chip Toggle Generators to Provide Realistic Conditions During Test of Digital 2D-SoCs and 3D-SICs

5.3 A PVT-Resilient No-Touch DFT Methodology for Prebond TSV Testing

SESSION 6
Security Track: Hardware Trojans

6.1 Scalable Hardware Trojan Activation by Interleaving Concrete Simulation and Symbolic Execution

6.2 Detection of low power Trojans in Standard Cell Designs Using Built-in Current Sensors.

6.3 Hardware Dithering: A Run-Time Trojan Neutralization Method for Wireless Cryptographic ICs

☆Distinguished Paper

Click here to see session chairs and presenters.

SPECIAL SESSION 2
Embedded Tutorial
Analog Fault Simulation: Practical Applications, Case Studies and Challenges

Case studies on actual analog IPs demonstrating several applications in design and manufacturing (coverage, defect based test, diagnosis, test optimizations, sensitivity analysis, etc.) will be presented.

SESSION AI 3
Machine Learning in Yield Learning

AI 3.1 Machine Learning for Yield Learning and Optimization

AI 3.2 Practical Applications of Big Data Analytics in Semiconductor Manufacturing, Assembly and Test

10:30 a.m. – 12:00 p.m.

SPECIAL SESSION 3
Testing of Gigascale Designs

S 3.1 DFT Considerations and Flow for a Large 2.5D/3D Device

S 3.2 Test Challenges for Low Power SoCs

SESSION 7
Advanced and Emerging Devices

7.1☆ Built-In Self-Diagnosis and Fault-Tolerant Daisy-Chain Design in MEDA Biochips

7.2 Analysis of Process Variations, Defects, and Design-Induced Coupling in Memristors

7.3 DPPM Reduction Methods and new Defect Oriented Test Methods Applied to Advanced FinFET Technologies

SESSION 8
Security Track: Securing HW and DFT

8.1 TimingSAT: Decamouflaging Timing-based Logic Obfuscation

8.2 IJTAG Integrity Checking with Chained Hashing

8.3 Pre-silicon Formal Verification of JTAG Instruction Opcodes for Security

SESSION AUTOMOTIVE 1
Case Studies of Automotive SOCs.

Auto 1.1Test Application and Evaluation Methods to Meet Run-time Self-test Requirements for Functional Safety

Auto 1.2 Advanced Uniformed Test Approach for Automotive SOCs

Auto 1.3 Case Study and Advanced Functional Safety Solution for Automotive SOCs

SESSION 9
Machine Learning in Test and Diagnosis

9.1 Improving Diagnosis Efficiency via Machine Learning

9.2 Artificial Neural Network Based Test Escape Screening Using Generative Model

9.3☆ Concept Recognition in Production Yield Data Analytics

Security Track | AI Track | Automotive Track

Wednesday Afternoon

2:00 p.m. – 3:30 p.m.

ITC INDIA SESSION
Top Three Papers from ITC India 2018

ITC-India 1 Improved RAM Sequential Tests for SoCs with Complex Memory Architectures

ITC-India 2 High-Accuracy, Robust Multiple-Defect Diagnosis Scheme

ITC-India 3 Enhancing Automotive Self-Test with Embedded Distributed Programming

SESSION AUTOMOTIVE 2
Panel: Automotive Functional Safety

Click here to see panel description and panelists.

AI 4
AI and Autonomous Machines

AI 4.1 An Autonomous System View to Apply Machine Learning

AI 4.2 Design Automation for Intelligent Automotive Systems

SESSION 10
Security Track Session: Trust but Verify

10.1 Hardware IP Trust Validation: Learn (the Untrustworthy), and Verify

10.2 EMFORCED: EM-based Fingerprinting Framework for Counterfeit Detection with Demonstration on Remarked and Cloned ICs

10.3 Barricade Methodology for Detecting Counterfeits
J. Bellay, Battelle

Free
Exhibits Admission
Tuesday,
Wednesday and
Thursday
also visit
ISFTA *exhibits*

Click here to see session chairs and presenters.

9:00 a.m. – 10:30 a.m.

SESSION 11
Novel Diagnosis Approaches

11.1 An effective methodology for automated diagnosis of functional pattern failures to support silicon debug

11.2 Improving Diagnosis Resolution and Performance at High Compression Ratios

11.3 Online Scan Diagnosis - A Novel Approach to Volume Diagnosis

SESSION 12
Communication and Interface Testing

12.1 Polynomial Chaos modeling for Jitter estimation in high-speed links

12.2 Self-Learning Health-Status Analysis for a Core Router System

12.3 A Stressed Eye Testing Module for Production Test of 30-Gbps NRZ Signal Interfaces

SPECIAL SESSION 5
Beyond System Test

S 4.1 Challenges of At-Speed testing of 112Gbps devices

S 4.2 Evolution of System-level Test at AMD

S 4.3 What Would It Take to Achieve Cost-Effective System-level Test?

SESSION 13
Analog Safety and BIST for Automotive

13.1 XLBIST: X-tolerant Logic BIST

13.2☆ Deterministic Stellar BIST for In-System Automotive Test

13.3 Improving Analog Functional Safety Using Data-driven Anomaly Detection

Click here to see session chairs and presenters

SESSION AI 5
AI-Enabled ATE

AI 5.1 AI Engineering Assistants for ATE

AI 5,2 Is It Possible to Impact Quality of Test with Machine Learning?

AI 5.3 Moving Adaptive Test to "AI Test"

1:30 p.m. – 3:00 p.m.

SPECIAL SESSION 6
Advanced Memory

S 5.1 Defect Injection, Fault Modeling and Test Algorithm Generation Methodology for STT-MRAM

S 5.2 Testing Resistive Memories: Where We are Standing and What Is Still Missing?

SPECIAL PANEL
ITC 50—Past, Current, and Future

Click here to see panel description and panelists.

AUTOMOTIVE 3
Imbedded Tutorial: Automotive Reliability

Auto 3.1 Modeling and Testing of Aging Faults in FinFET Memories for Automotive Applications

Auto 3.2 ECC-Based FIT Rate Mitigation Technique for Automotive SoCs

AI PANEL
Could AI Eliminate the Need for Test Engineering?

Click here to see panel description and panelists.

Posters

W. Eklow, Retired (Chair/Coordinator)

PO1 IEEE 1149.1-2013 Intel Product Compliance and Industry Enablement Plans
P. Chen, J. Grealish, Intel

PO2 § A Functional Approach to Test and Debug of IEEE 1687 Reconfigurable Networks
M. Portolan, R. Cantoro, E. Sanchez, M. Reorda, Politecnico di Torino

PO3 Interpreter of MATLAB/Simulink MAT-Output Files for Use As Test and Verification Stimulus for Verilog Simulations with Cadence NCSim.
T. Klotz, M, Versen, Hochschule Rosenheim

PO4 Run-Time Aging Prediction Through Machine-Learning
K. Kannan, M. Portolan, L. Anghel, Grenoble-INP/TIMA

PO5 New Standard Test Interface Language (STIL) Applications.
E. Wahl, HiTestWare

PO6 § Dynamic Cloud-based Data Collection System.
G. Lawton III, Lawton Software

PO7 § Layout-aware Wrapper for IP cores D. Patel (AMD) and K. Agarwal , AMD

PO8 § IEEE P1687.1: Extending 1687 to Non-TAP Interfaces.
J. Rearick, AMD, A. Crouch, Amida, M. Keim, Mentor, A Siemens Business, M. Laisne, Dialog Semi, G. Colon-Benet, Intel

PO9 § Visually-enhanced Dynamic Part Average Testing.
A. Coyette, R. Vanhooren, W. Dobbelaere, ON Semiconductor, B. Esen, N. Xama , J. Caicedo, G. Gielen, Katholieke Universiteit Leuven

P010 Non-Contact Probing for Electrical Connectivity of Printed Circuits
J. Kang, K Chae. Samsung

PO11 IJTAG Security
J. Johnson, B. Atwell, SiliconAid Solutions, A. Crouch, Amida

PO12 IEEE 1687 (IJTAG) Evolution
J. Johnson, B. Atwell, SiliconAid Solutions, A. Crouch, Amida

PO13 § Concurrent IJTAG
R. Krenz-Baath,HSHL

PO14 Are You Really Testing Your Memory? Automating Test and Verification of All Memory Functionality
J. Hung, Microsoft, V. Neerkundar, Mentor, A Siemens Business

PO15 § IEEE P1687.2: Extending 1687 to Analog Circuits
J. Rearick, AMD, S. Sunter, Mentor, A Siemens Business, V. Zivkovic, Cadence

PO16 In-system and Manufacturing Test Flow for Large Automotive ICs
K. Subramanian P. Jaini, Ambarella, A. Arozqueta, M. Abdelwahid, Mentor, A Siemens Business

PO17 On Generating Fault Diagnosis Patterns in the Presence of Xs
X. Lin, Mentor, A Siemens Business, S. Reddy, University of Iowa

PO18 Enabling High Quality Silicon with Collaboration of Post Silicon Validation and Systems.
V. Achari, S. Chaudhry, Texas Instruments

PO19 Tester Board Tracking System Using Streaming RITdb.
S. Ajouri, D. Foreman, Texas Instruments

PO20 ATE Not Required: A Complete Test Solution to Accelerate First-Silicon Shipping of a Large AI Design
J. Ferguson, P. Freeman, Graphcore, P. Hudson, L. Harrison, Mentor, A Siemens Business

PO21 Effective Testing of Identical Hierarchical Cores
V. Neerkundar, R. Press, Mentor, A Siemens Business

PO22 § Optimal SCAN Vector Count
T. Kogan, A. Rabenu, Intel

PO23§ What's up with Analog Test Coverage?: IEEE P2427 IEEE Working Group Progress.
A, Meixner, The Engineers' Daughter, S, Abdennadher, Intel), S, Sunter, Mentor, A Siemens Business, P. Sarson, Dialog Semiconductor

PO24 An Improvement of Routability of Memory Test Interface Board by Auto Pin Assignment Algorithm
M. Yang, A. Fan, A. Huang, Advantest

PO25 TAP-based Scan Testing of High-Performance Image Sensor Chip
J.Sanchez, ON Semiconductor, R. Singhal, Mentor, A Siemens Business

PO26 Error Sources to Trim Distributions
H. von Staudt, Dialog Semiconductor

PO27 Discrete-Time Controller Implementation for Automotive High-Reliability Testing
K. Fan, Advantest Taiwan

PO28 § Method to Measure and Improve Toggle Coverage During High-Volume Quick-Kill Stress
J. Cooper, Intel

PO29 Low-Pin-Count Testing of an Industry Transceiver Chip.
R. Singhal, Mentor, A Siemens Business, I. Ahmed, Qualcomm, S. Baraiya, Qualcomm India

PO30 Influence of Machine Learning on Post-Silicon Validation and Analysis.
V. Achari, Texas Instruments, S. Achari ,V. Kutty, soliton technologies

PO31 Cancelled

PO32 Novel IJTAG and IJTAG.1 Architecture Alternatives
M. Luiz, H. von Staudt), B, Vasu, D. Cioaca, Dialog Semiconductor

PO33 Metal-Oxide (MOX) Gas Sensor Testing
D. Johnson, M. Dewey, Marvin Test Solutions

PO34 Analog Test Bus for High-Precision, High-Speed Parallel Measurement of Test Point Voltages Distributed over Multiple IPs
J. Schat, R. Jin, L. Ma, NXP Semiconductors

PO35 STAM - Reusing Device Access for Board and System Test
I. McIntosh, Leonardo MW; H. Ehrenberg, GOEPEL Electronics

PO36 Built-in Fault Injection and Detection for Safety-Critical IC
J. Schat, X. Hours, A. Barrilado, NXP Semiconductors

PO37 One of the Ways Further to Step into Autonomous Driving
J. Schat, U. Möhlmann , NXP Semiconductors

§ Top 10 Poster

Panels

Monday, 4:45 p.m. – 6:15 p.m.

PANEL 1 Physical Inspection and Attacks: New Frontiers in Hardware Security

M. Tehranipoor, University of Florida (Moderator)

Globalizing electronic component and systems supply chain has raised serious concerns about security and trust. This panel discusses security issues in integrated circuits and systems, and present physical inspection methods to detect malicious change and fake parts. It also discusses new physical attacks enabled by advances in instruments.

Panelists *C. Boit*, TU Berlin • *Y. Iskandar*, Cisco Systems • *Y. Jin*, University of Florida • *D. Lam*, MultiBeam • *E. Principe*, Synchotron Research

A social reception will be held at 6:30 p.m. following Panel 1.

Wednesday 2:00 p.m. – 3:30 p.m.

Automotive 2 Panel: Automotive Functional Safety: How Much Is Enough?

P. Bernardi, Polito Torino (Moderator)

This panel will discuss the implications of automotive functional safety requirements on all aspects of the SOC design, manufacturing quality and particularly in-system functional safety, such as power-on self-test, periodic self-test, etc. This panel will discuss the range of such solution for different categories of automotive SOCs.

Panelists *N. Bishnoi*, GLOBALFOUNDRIES • *C. Eychenne*, Bosch • *N. Maor*, Qualcomm • *R.Mariani*, Intel
R. Srinivasan, NVIDIA • *Y. Zorian*, Synopsys

Thursday 1:30 p.m. – 3:00 p.m.

SPECIAL PANEL ITC 50—Remember the Past and Imagine the Future

In 2019, ITC will enter its 50th year. In these 50 years, ITC has gone through many stages and changes. As ITC reaches this significant milestone, what do you see our community has become and should be moving forward?

Panelists *The 2019 ITC 50 organizing committee and a few other past chairs would like to hear your thoughts.*

AI PANEL Could AI Eliminate the Need for Test Engineering?

R. Aitken, ARM (Moderator)

Following the AI mini-keynotes in the morning, this afternoon panel provides a forum to have more in-depth discussion. AI has become an inevitable force to affect many industries. How do we see AI might transforms our industry? The most extreme question perhaps is: Will AI eventually eliminate test engineering? If not 100%, to what extent and when? There are many questions surrounding AI and most importantly, do we really understand what AI is? After hearing different perspectives in the morning, come and share your thoughts in this panel.

IEEE Computer Society Test Technology Technical Council Workshops

Thursday and Friday

General Workshop Information

Three workshops are being held in parallel immediately following ITC 2018. They will each start with an opening address on Thursday afternoon, November 1, followed by a technical session. A reception for all workshop participants will be held on Thursday evening. The remaining the technical sessions will be held on Friday, November 2. The technical scope of each workshop is described below.

Workshop Registration

All workshop participation requires registration. To register in advance for one of the workshops, do so online or by contacting the ITC office for a paper registration form. Otherwise, register onsite at the **ITC registration counter** in the **Phoenix Convention Center North Hall** during Test Week**.** Admission for onsite registrants is subject to availability. Discount workshop registration rates apply until October 8, 2018. See page 26 for details. Workshop registration includes the opening address, technical sessions, digest of papers, workshop reception, break refreshments, continental breakfast and lunch.

Digest of Papers

A digest of papers will be distributed only to attendees at the workshops as an informal proceedings.

Workshop Schedule

The three workshops will adhere to the same schedule:

Thursday, November 1		Friday, November 2	
Registration	2:00 p.m. – 5:00 p.m.	Registration	7:30 a.m. – 10:00 a.m.
Opening Address	4:00 p.m. – 4:30 p.m.	Technical Sessions	8:00 a.m. – 4:00 p.m.
Technical Session	4:30 p.m. – 6:30 p.m.		
Reception	7:00 p.m. – 9:00 p.m.		

Note: Workshop schedule is subject to change

Further Information

For more information on the workshops contact their organizers by e-mail or check the TTTC Web site http://ieee-tttc.org

WORKSHOP RECEPTION

Thursday, November 1
Hyatt Atrium 2
7:00 p.m. – 9:00 p.m.

ART 2018: 3rd IEEE International Workshop on Automotive Reliability and Test

Scope: The ART workshop focuses exclusively on test and reliability of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration and in-field test, diagnosis and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety, and cost. constraints of a mass market, the reliable operation of electronics in safety-critical domains is still a major challenge. This third edition of the ART workshop offers a forum to present and discuss these challenges and emerging solutions among researchers and practitioners alike.
The scope of the workshop includes, but is not limited to:

- Functional safety and security in the automotive domain
- Automotive standards and certification – ISO 26262
- Approximate computing and artificial intelligence
- Multilayer dependability evaluation
- Verification and validation of automotive systems
- Fault tolerance and self-checking circuits
- Aging effects on automotive electronics
- Resiliency by application
- Dependability challenges of autonomous driving and e-mobility
- Power-up, power-down and periodic test
- System level test
- Reuse of test infrastructure
- Functional and structural test generation
- High quality volume test- minimizing DPPM life-cycle test cost minimization

General Chair: Yervant Zorian zorian@synopsys.com
Program Chair: Paolo Bernardi paolo.bernardi@polito.it

TVHSAC: 5th IEEE International Workshop on Test and Validation of High-Speed Analog Circuits

Scope: The IEEE Workshop on Test and Validation of High-Speed Analog Circuits (TVHSAC) is a forum to address the pre-silicon and post-silicon validation, manufacturing test, in-field reliability and security challenges in analog, mixed-signal and RF circuits and systems for high-speed applications. Topics include:

- Built-in test and design-for-test
- Self-healing, self-calibration and self-adaptation techniques
- Sample selection for pre-silicon and post-silicon validation
- Behavioral modeling
- Efficient mixed-signal simulation
- Analog fault modeling and fault simulation
- Analog and mixed-signal diagnosis
- Reliable and secure AMS circuit design
- Test access mechanism
- Analog test bus design
- SERDES test and characterization
- RF circuits test and characterization
- High speed data converter test and characterization
- High speed PLL test and characterization
- Precision delay-line test and characterization
- Clock jitter and skew measurement
- Phase noise measurement
- AC and DC supply noise measurement
- ATE technology
- Board technology
- Economics of test and yield optimization

General Chair: Ke Huang, khuang@sdsu.edu
Program Chair: Manuel Barragan, manuel.barragan@imag.fr

SPDT: IEEE International Workshop on Silicon Photonics Design and Test

Scope: IEEE International Workshop on Silicon Photonics Design and Test focuses exclusively on design and test of silicon photonics systems, including design, EDA tools, manufacturing, as well as architectures and co-design methods to integrate silicon photonics into traditional electronics systems. In the emerging data center, cloud computing and high-performance computer eras, silicon photonics is a key enabler. SPDT offers a forum to collaborate the silicon photonics experts with electrical design and test researchers and practitioners to present and discuss these challenges and emerging solution. Topics include:

- Photonic IC design
- Tools
- Wafer-level test
- Manufacturing
- Sensors
- LiDAR
- Transceivers
- Biomedical
- Switches

General Chair: Yinchieh Lai, yelai@mail.nctu.edu.tw
Program Chair: Jyehong (Jason) Chen, jchen@mail.nctu.edu.tw

ITC Receptions

Monday 6:45 p.m. – 8:15 p.m.

ITC Post-Panel Social

Monday, October 29, 6:15 p.m. – 8:00 p.m.

Enjoy a networking gathering following the panel, with beer/wine and appetizers.

Tuesday 5:30 p.m. – 7:30 p.m.

ITC Welcome Reception

Jointly with ISFTA

Tuesday, October 30, 5:30 p.m. – 7:15 p.m.

Phoenix Convention Center North Hall

Join with colleagues and friends for an evening of food and libations.

Registration Categories

Register Online *or* Contact the ITC Office for a Registration Form

All Test Week activities require a registration badge for admittance. There are three registration periods with differing fees

- Early discount preregistration through October 8, 2018
- Nondiscount preregistration October 9 to October 21, 2018.
- Onsite starting October 22, 2017

Online registration is the preferred preregistration mode prior to the conference. Onsite registration takes place at the **ITC registration counter** at the **Phoenix Convention Center North Hall.** See page 27 for registration hours. To obtain a **substantial discount** register no later than October 8, 2018.

▶ITC Full-Conference Registration Includes ITC technical paper and panel sessions, exhibits, ITC welcome reception, lunch in the exhibit hall, break refreshments, download ITC 2018 Proceedings and Technical Presentations and ITC giveaways. Registration does not include the tutorials on Sunday and Monday or the workshops on Thursday and Friday. You may purchase additional download ITC 2018 Proceedings at $25 each.

▶ITC One-Day Registration (Onsite-only) Includes ITC technical program activities, exhibits, lunch in the exhibit hall and break refreshments—all for the day of registration only. Also includes ITC 2018 Proceedings and Technical Presentations and ITC giveaways. Registration does not include ITC welcome receptions. You may purchase: additional download ITC 2018 Proceedings at $25 each

▶ITC Free Exhibits-only Registration (Onsite or Online) Includes admission to exhibits on Tuesday, Wednesday and Thursday and corporate presentations on Tuesday. Lunch and ITC receptions and giveaways are not included.

▶Student Rates IEEE student members must also present their current IEEE Student Member card at the ITC registration counter. Student nonmembers must present their current school student ID.

▶Tutorial Registration Tutorials are a half-day in length.
One-Day tutorial registration fee is for two tutorials—a morning tutorial and afternoon tutorial, both on the same day, e.g., Tutorial 1 and Tutorial 4 on Sunday. You may register for up to four tutorials (two consecutive on Sunday and two consecutive on Monday).
All-Access Pass tutorial registration provides in-and-out access to all twelve tutorials over both days.

All registrations include study material, breaks and lunches on the day(s) attended. Tutorial registration does not include the ITC technical program, ITC receptions, exhibits, exhibit hall lunches, ITC publications, ITC giveaways or the workshops on Thursday and Friday.

▶Workshop Registration Includes the items specified on page 22. Registration does not include the ITC technical program, exhibits, ITC receptions, exhibits, exhibit hall lunches, publications, ITC giveaways or the tutorials on Sunday and Monday.

▶Discount Rates Early registration rates apply only when you complete your registration by September 30, 2018, either online or with a paper form and payment postmarked or faxed by October 16, 2016\8. To receive IEEE member or student member reduced rates, you must include your member number, which will be verified.

▶Co-Located ISTFA Events There are many opportunities for registered ITC attendees to participate in ISTFA events. Click here to see details. In addition, ITC full-conference registrants may purchase ISTFA full-conference registration onsite for the discounted fee of $350.

Registration Fees

Registration Fees

Early Discount Preregistration Fees*	Full ITC Conference	1-Day-only Conference†	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE Member	$795	n.a.	$225	$550	$240
Nonmember	$995	n.a.	$282	$664	$300
IEEE Student and Life Member	$270	n.a.	$225	$550	$130
Nonmember Student	$340	n.a.	$282	$664	$240

* Not available after October 8, 2018
† Available onsite only.

Regular Preregistration Fees**	Full ITC Conference	1-Day-only Conference†	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop
IEEE Member	$1035	n.a.	$282	$664	$300
Nonmember	$1295	n.a.	$428	$976	$375
IEEE Student and Life Member	$270	n.a.	$282	$664	$160
Nonmember Student	$340	n.a.	$428	$976	$300

** Available October 9, 2018 to October 21, 2018
† Available onsite only.

Late/Onsite Fees***	Full ITC Conference	1-Day-only Conference†	One Day 2 Tutorials	All-Access Tutorial Pass	One Workshop	Full ISTFA Conference††
IEEE Member	$1140	$355	$282	$664	$300	$350
Nonmember	$1425	$445	$428	$976	$375	
IEEE Student and Life Member	$270	n.a.	$282	$664	$160	
Nonmember Student	$340	n.a.	$428	$976	$300	

***Starting October 22, 2018
† Available onsite only.
†† Available onsite only for ITC full-conference registrants.

Refunds

All refund/cancellation requests must be provided in writing and received by October 9, 2018. No refunds will be issued after October 9, 2018. Please submit all refund/cancellation requests to: ITC2018@badgeguys.com. There will be a cancellation fee of $75 and will be deducted from each refund..

Registration Hours

Registration for Tutorials

ITC registration counter at the Hyatt Regency Phoenix
Sunday, October 28
7:30 a.m. – 10:00 a.m.

Registration for All Activities

ITC registration counters at the Phoenix Convention Center North Hall, third floor.
Sunday, October 28 11:00 a.m. – 5:00 p.m.
Monday October 29 to Thursday, November 1
7:30 a.m. – 5:00 p.m.

Need More Registration Information?

Contact the ITC office
2025 M Street, NW, Suite 800, Washington, DC 20036, USA
Tel. +1 202.973.8665 Fax. +1 202.973.8716

ITC 2018 Proceedings Distribution

ITC proceedings will be delivered electronically.

All ITC full-conference and one-day attendees, including students, will receive access to the ITC online proceedings free of charge.

Preregistered Full-Conference Attendees
All preregistered full-conference attendees will receive an email containing a download link a few days before the conference when the proceedings become available.

Onsite Full-Conference and One-Day Attendees
Full-conference and one-day attendees registering onsite will receive the download link at the time of registration.

ISTFA Attendees at ITC
ISTFA attendees who purchase the $350 full-conference ITC registration onsite will receive the download link at the time of registration.

Ordering Additional Proceedings with Advance Registration
All preregistered full-conference attendees may also order additional download 2018 proceedings, beyond the free copy, at $25 each.

Purchasing Additional Proceedings at the Conference
Full-conference and one-day attendees may also purchase onsite additional downloads of the 2018 proceedings for $25 each.

ITC 2018 Technical Paper Presentations

Available free for download along with proceedings.

The ITC Program Committee has compiled the slides used for this year's technical paper presentations—including invited presentations—and has them available for download*. You can review sessions that you attended and cover those that you could not attend. This will only be available as a free download to registered full- and one-day conference attendees, including students—one per person. Preregistered attendees will receive a download link a few days before the conference. Others will receive the link when they register onsite.

The paper presentation slides make the perfect complement to the full manuscripts in the proceedings, as they contain the latest data .

*Some authors have chosen not to participate. These omitted papers will be identified. Slides used in panel sessions and the corporate forum are not included.

Online Hotel Reservations

Reserve a Phoenix room online from our **only** official housing vendor by clicking the button above.

- Rooms may be reserved through September 27, 2018 at the ITC rate.
.
- Cancellations: reservations must be cancelled no later than 3:00 p.m. location time, 72 hours prior to the date of arrival to avoid a one night's room fee and tax penalty.

- The reservation cutoff date for booking at the ITC rate is **September 27, 2018.** Reservations made after this date will be made at the ITC rate on a space-available basis. Contact jay@connectionshousing.com

- Parking: hotel valet parking $33 per day and discounted self-parking nearby at $17.25. Prices subject to change without notice, plus tax.

- Internet access is complimentary in all guest rooms.

- If you need assistance to reserve 1-9 rooms, contact **Connections Housing** at 404-842-0000 or 800-262-9974 and a call-center agent will assist. For 10 or more rooms, email jay@connectionshousing.com or call 404-918-9129.

Hyatt Regency Phoenix
122 N. Second Street
Phoenix, AZ 85004
Phone: 602.252.1234

USD 209.00 Average nightly rate +12.5% tax*

*Tax subject to change without notice,

Message to Attendees: ITC has made every effort to secure the best possible group nightly room rate for you at this event. That rate results from a negotiated overall package of event needs such as sleeping rooms, meeting room space and other requirements. Contracts with the venue include a provision to reduce event costs if ITC meets or exceeds its minimum sleeping room block guarantee. Conversely, event costs will increase if ITC falls short of its minimum room block guarantee. Please help ITC keep the costs of this event as low as possible by booking your housing needs at the designated host hotel and through the reservation process created by ITC. Reserving elsewhere means you are booking outside the contracted room block, jeopardizing ITC's ability to meet its contracted obligations and to keep registration fees to a minimum. ITC appreciates your support and understanding of this important issue. Thank you.

Location & Travel

Location

ITC and the co-located ISFTA conferences and all associated ITC Test Week events will be held at either Phoenix Convention Center North Hall in downtown Phoenix or the Hyatt Regency host hotel, which is close to the convention center

The city of Phoenix and the surrounding areas feature cultural, shopping and scenic attraction too numerous to mention here. For a comprehensive overview, visit the Phoenix Convention and Visitor's Bureau site.

.

Travel

Air
Phoenix is serviced by the Skyharbor International Airport (PHX) which is about four miles road miles from the Phoenix Convention Center. There are several transportation options from the airport to downtown Phoenix including: taxi, shared vans and public transportation.

SuperShuttle Shared Van
We have established a 10% discount for Super Shuttle shared vans and ExecuCar sedans and SUVs for airport transfers during ITC. The link below will take you to the site where reservations can be made. International Test Conference Discount Link**.** The fare before discount is approximately $18 by van.

Taxi
Taxi service from PHX is available for a rate of about $25.

Car
Driving directions to the Hyatt Regency, which is across the street from the convention center.

Information

1. The ITC Advance Program release 8.0 was generated with Adobe Acrobat 8.2.6 on 23-October-2018

2. The program will be updated periodically as new material is available—check back often.

3. Navigate using the tabs and links at the top of each page.

4. Use underlined links in the At-a-Glance to find specific items.

5. For more information contact:

Subject	Contact	Email
Advance Program	Don Denburg	denburg@rcn.com
Corporate Forum	Rob Knoth	knoth@cadence.com
Exhibits and Exhibiting	Bill Lowd	bzintrnatl@aol.com
Fringe Technical Meetings	Courtesy Associates	itc@courtesyassoc.com
Hotels	Connections Housing	jay@connectionshousing.com
Posters	Bill Eklow	beklow56@gmail.com
Registration	Courtesy Associates	itc@courtesyassoc.com
Technical Program	Bill Eklow	beklow56@gmail.com
TTTC Tutorials	Yervant Zorian	zorian@synopsys.com
TTTC Workshops	Yervant Zorian	zorian@synopsys.com
All Other Questions	Courtesy Associates	itc@courtesyassoc.com

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media.

Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE.

Photographs of copyrighted PowerPoint or other slides are for personal use only and are not to be reproduced or distributed. Do not photograph any such images that are labeled as confidential and/or proprietary.